

# **MONITERM CORPORATION**

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## **OPERATING MANUAL**

## **VR-SERIES**



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## I. GENERAL

The Moniterm VR series display monitor utilizes the latest advances in integrated circuits and switching technology teamed with a high performance CRT. Horizontal frequencies are available from 32 KHZ to 68 KHZ and retrace times as low as 2.8 u seconds.

A separate modular high voltage supply allows wide variations in displayed video without changing brightness levels or display blooming, allowing the display designer to use visual attributes such as; reverse video, blink, and reverse blinking video without ill effects. This high voltage supply also allows a wide range of horizontal retrace times. This is very helpful in applications where the display drive logic has bandwidth limitations.

### Environmental

Temperature Range: Operating: 10C to 50C (50F to 122F)  
Transit storage: -40C to 85C (-40F to 185F)

Humidity: 5% to 90% (non-condensing)

Altitude: Operating: up to 10,000ft (3.0 km)

Transit Altitude: up to 40,000ft. (12.2 km)

### X-RADIATION

The monitors comply with DHEW standard 21-CFR-sub chapter J when the monitor is operated within the specified input voltage limits.

### WEIGHTS

VR-15-21

VR-17-27

VR-19-33

### FULL BODYSHIELD

VR-15 2.5 pounds

VR-17 4.0 pounds

VR-19 5.25 pounds

Low Voltage Power Supply: 6 pounds

Low Voltage Power Supply Shield: 1 pound

Geometric Distortion - sweep non-linearities and pin cushion distortion exceed the requirements of EIA STD RS-375A.

### Internal Controls (See Adjustment Section)

Horizontal width

Horizontal Hold

Horizontal Linearity

Horizontal Dynamic Focus

Vertical Hold

Vertical Size

Vertical Top Bottom Linearity

Vertical Linearity

Vertical D.C. Centering

Vertical Dynamic Focus

Final Anode Voltage

D.C. Focus

Brightness

Video Contrast

### Optional Controls

Remote Brightness: 100K 1/2watt potentiometer. With the remote brightness option the internal brightness control is a range control.

Remote Contrast: TTL Video 5K ohm 1 watt potentiometer  
ECL Video 500 ohm 5 watt potentiometer

## II. POWER INPUT

The monitor's power input connector is a Molex #22-27-2041 4 pin connector configured as follows:

Pin # 1	+48vDC
Pin # 2	GND
Pin # 3	GND
Pin # 4	+32vDC

\*For Power requirements see the power dissipation chart

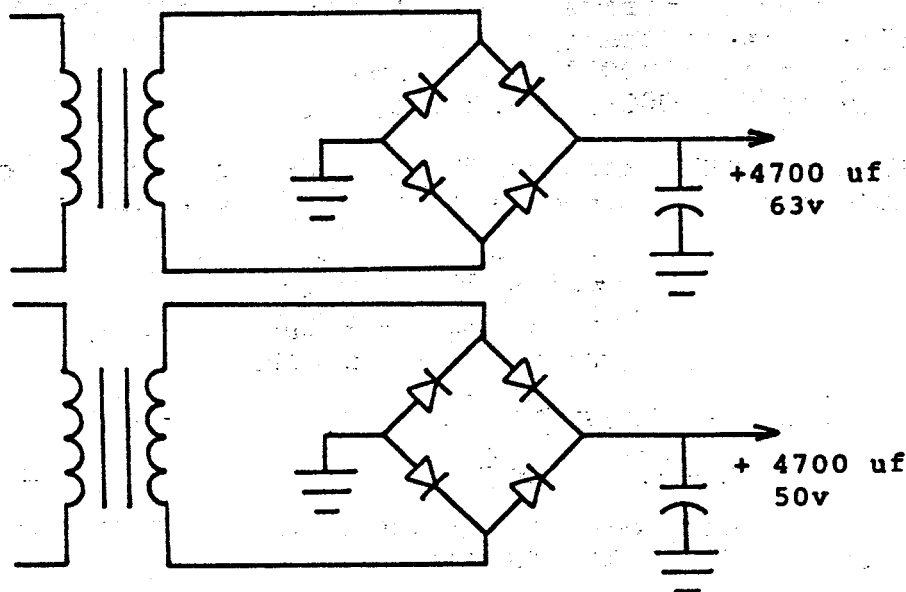
## III. MATING CONNECTOR

The power input connector should be mated to Molex #22-01-2045

The Molex pin for this connector is #08-50-0136

## IV. POWER SUPPLY CIRCUIT

Since the deflection board has on board regulators, the raw D.C. power circuit shown below is satisfactory.



## V. POWER DISSIPATION CHART

Average D.C. Power	15P	15L	17P	17L	20P	20L
+48v $\pm$ 10% (50 KHZ Horizontal)	875ma	1.0a	950ma	1.0a	950ma	1.1a
+32v $\pm$ 10% (50 KHZ Horizontal)	650ma	550ma	750ma	600ma	800ma	650ma
+48v $\pm$ 10% (64 KHZ Horizontal)	875ma	1.1a	950ma	1.1a	950ma	1.1a
+32v $\pm$ 10% (64 KHZ Horizontal)	650ma	550ma	750ma	600ma	800ma	650ma

Moniterm supplied low voltage power supply

Input voltage 100v, 120v, 220v, 240v, RMS 50/60 HZ  
programming card selectable

Input power 75w (nominal) See model chart

VI TTL INTERFACE SPECIFICATIONS  
(Connector Molex #09-75-1061)

Pin out

Vertical Sync	1
GND	2
Horizontal Sync	3
GND	4
Video (1 Banks)	5
GND	6

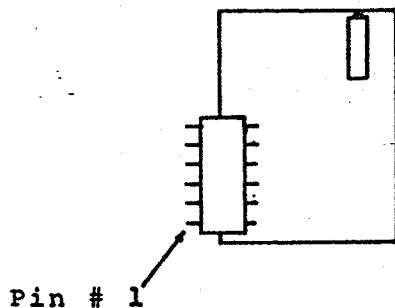
For Sync Specifications see separate Syncs

MATING CONNECTOR

Molex #09-50-3061

Molex Pin # 08-50-0106

Top of the TTL Board



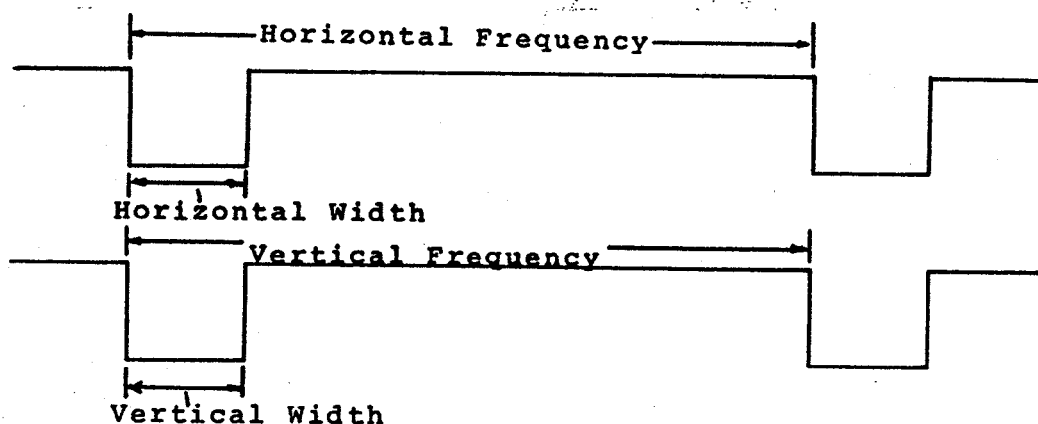
TTL VIDEO

<u>Amplitude</u>	<u>Input Impedance</u>	<u>Video Rise and Fall Time</u>
Low Level (0.0 to 0.8v)=white	220/330ohm Termination to +5v (130ohm)	4 n sec
High Level (+2.0v to +5.2v)=black		

## VII SEPARATE SYNC SPECIFICATION

	Amplitude	Input Impedence	Frequency	Width	Rise and Fall Time
Horizontal Sync	TTL compatible phase locks to negative edge LL=0.0 to 0.8v HL=2.0 to 5.2v	220/330ohm termination to +5v (130ohm)		150ns-5us	TTL comp.
Vertical Sync	TTL compatible negative edge Sync LL=0.0 to 0.8v HL=2.0 to 5.2v	220/330ohm termination to +5v (130ohm)	45-65HZ* (other frequencies available as an option)	100ms-300ms	TTL comp.

\* If a refresh rate of anything other than 60.0HZ is chosen the low voltage power supply transformer must be shielded with a mumetal shield to prevent a vertical swim problem in the monitor. For countries with 50HZ power, the refresh rate must be 50HZ to prevent the same problem.





# VIII ECL INTERFACE SPECIFICATIONS

Specifications: Logic levels shown below gives video on=white,  
reverse levels for video off=black

## Signal

## Connector

Most significant ( $2^2$ ) bit outer shell  
is high (-.96v to -.81v)  
Center is low (-1.85v to -1.65v)

J1

Second most significant ( $2^1$ ) bit outer  
shell is High (-.96v to -.81v)  
Center is low (-1.85v to -1.65v)

J2

Least significant ( $2^0$ ) bit outer  
shell is high (-.96v to -.81v)  
Center is low (-1.85v to -1.65v)

J3

J1,J2,J3, are BNC connectors

## ECL VIDEO

<u>Amplitude</u>	<u>Input Impedance</u>	<u>Video Bandwidth</u>	<u>Rise and Fall Time Video Amp</u>
Center conductor (-1.85v to -1.65v)	75ohm without -2v or -5.2v Pulldown	82 MHZ	(10% to 90%) 4.5n sec

Outer shell  
(-.96v to -.81v)

Logic levels above video on = white  
Reverse levels for video off = black

### IX SEPARATE SYNCs - ECL VIDEO BOARD

Signal	Connector Molex (#09-75-1061)J7	Amplitude	Input impedance
Vertical Sync Input	1	TTL compatible negative edge sync	120/180 ohm termination to +5v (72ohm)
GND	2		
Horizontal Sync Input	3	TTL compatible Phase locks to neg. edge	120/180ohm termination to +5v (72ohm)
+5v output (100ma max)	4		
GND	5		
-5v output (100ma max)	6		
<u>J7 Mating connector</u>			

Molex # 09-50-3061

Molex Pin # 08-50-0106

See silkscreen drawing for connector layout

See separate syncs page for sync specifications

See ECL interface page for video specifications

### X COMPOSITE SYNC - ECL VIDEO BOARD

Signal	Connector	Amplitude	Input impedance
Vertical Sync & Horizontal Sync	(BNC)J4	TTL compatible *LL=0.0 to 0.8v *HL=+2.0 to +5.2v	120/180 ohm termination to +5v (72ohm)

\*Low Level \*High Level

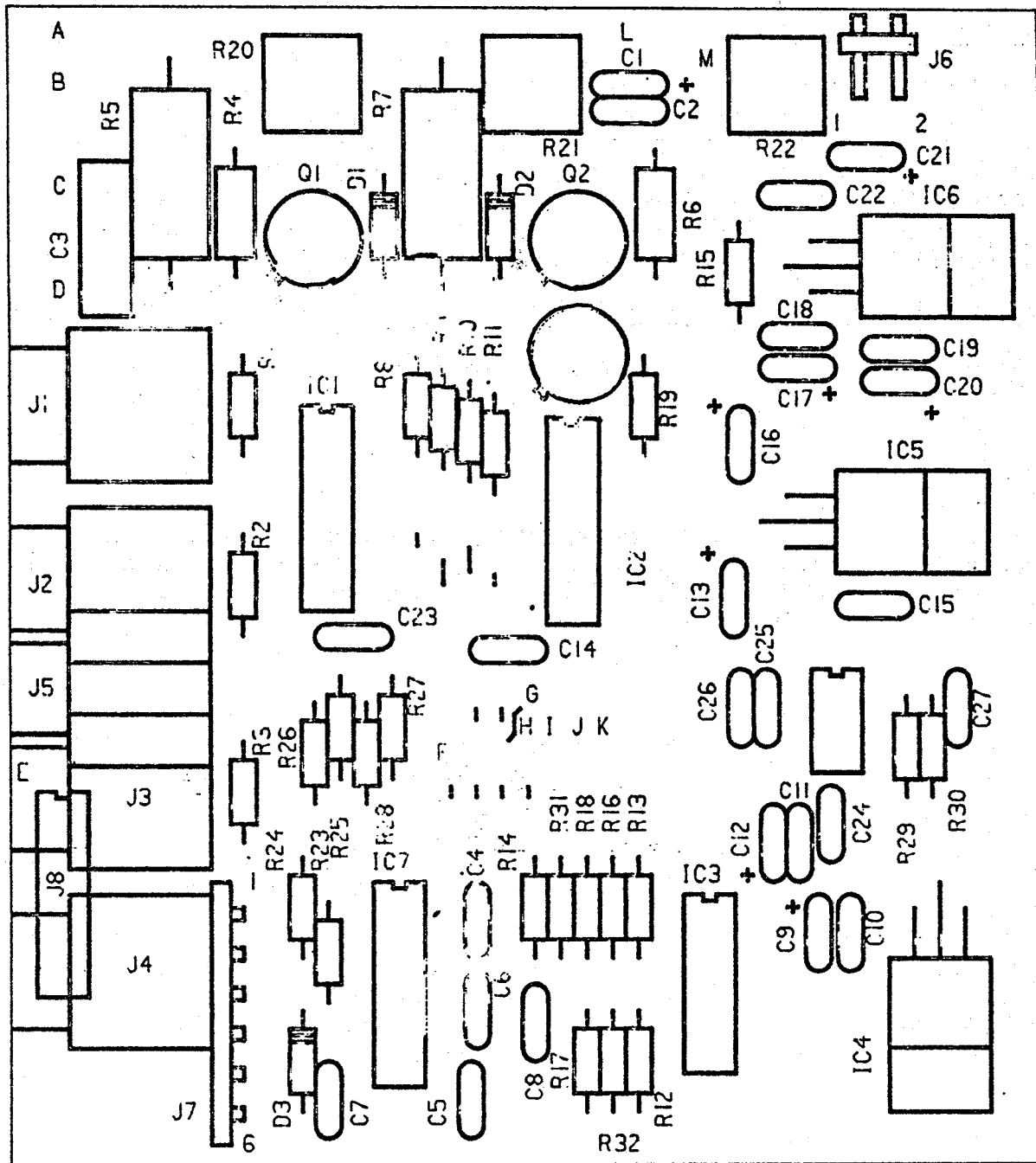
See composite Sync wave form

### XI TWO LEVEL COMPOSITE VIDEO

Signal	Connector	Amplitude	Input impedance
Two level composite video	(BNC) J4	Video-Two comparators adjustable from +2.5v to -3.5v Sync-comparator adjustable from +3.5v to -3.5v	75ohm to GND DC coupled

See Two Level Composite Video Option write up

# XII ECL BOARD ASSEMBLY



DTL820501 SILKSCREEN

## SECTION B DISPLAY TIMING

### I Horizontal Timing

The Monitorm Specification includes "back porch" retrace and "front porch" intervals. Since the retrace is phase locked to the falling edge of the sync pulse, and actually starts slightly before it, at least one blank character after the last display character position is recommended. Delaying the horizontal sync additional time causes the display to shift left; thus the user can center the display external to the monitor.

<u>Horizontal Scan</u>	<u>Retrace Time</u>	<u>Video Time</u>
64KHZ + 5%	*3.5 u sec max	11.5 u sec
50 KHZ +5%	*5 u sec max	15 u sec

\*These retrace times are maximum numbers. Since we are using a regulated High Voltage supply, faster retrace times are available. The retrace time and horizontal frequency can be customized to the customer's requirements.

### II Vertical Timing

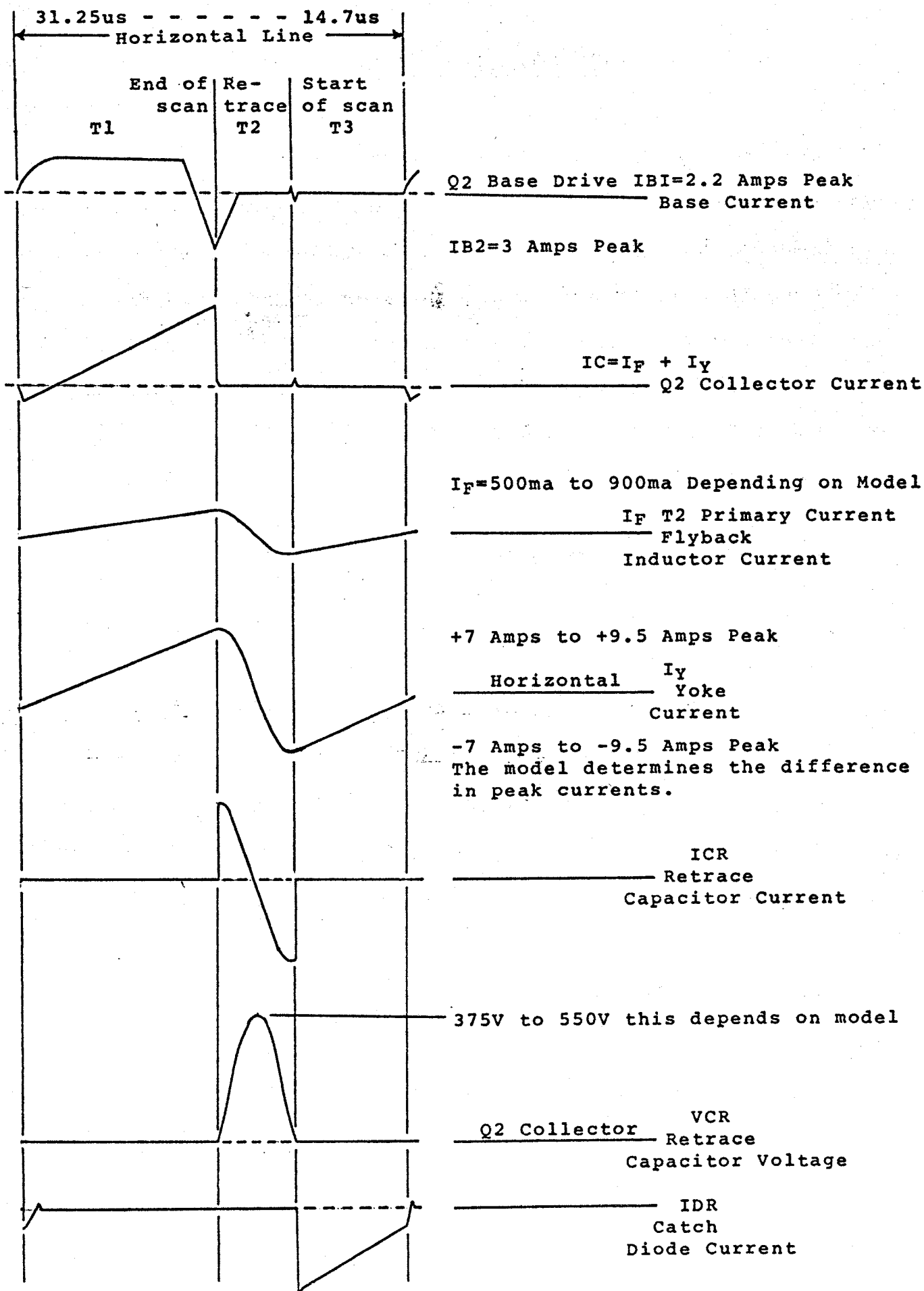
The vertical retrace is initiated on the falling edge of the vertical sync. Best results are obtained if this coincides with the horizontal sync or occurs during horizontal sync. For an interlaced display on alternate frames vertical sync is delayed one half the horizontal time, 7.5us for a 64KHZ horizontal. In any case, total vertical refresh should be a discrete function of the horizontal scan.

The vertical retrace interval is specified at 667us of which approximately 1/2 is beam retrace and 1/2 is settling time. The display is blanked only during the retrace interval. The additional raster lines are available for display although non-linearities are present.

Vertical sync can occur immediately after the last scan of the last display row. Delaying vertical sync additional scan times causes the display to move upward which can facilitate vertical centering or a very smooth scroll, raster by raster (panning).

The vertical oscillator free runs and is factory preset at 7% lower than nominal and will sync to signals initially + 7% from nominal. As with the horizontal setting, any unit for utilization at other than 60HZ should be specified so that vertical lock can be assured.

For the height, sync, and linearity adjustments, see the adjustment section.

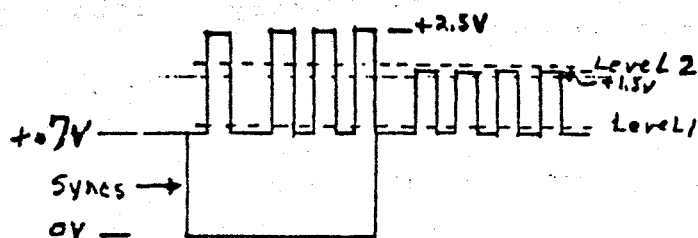


### III TWO LEVEL COMPOSITE VIDEO OPTION

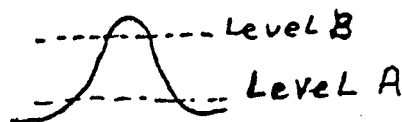
The Two Level Composite Video Interface uses an ECL comparator to sense two discrete video levels. These two levels are set by potentiometers R20 and R21 and can be adjusted between +2.5 to -3.5V.

The Sync is also sensed by a comparator and adjusted by potentiometer R22. The level may be adjusted between +3.5 to -3.5V.

To adjust the Video Comparators, set channel 1 to Video and channel 2 to D.C. potentiometer level. IC7 pin 5 is Level 1 and IC 7 pin 11 is Level 2.



For the example shown, Level 1 would be adjusted to +0.7 V plus the noise level. Level 2 would be +1.5 V plus the noise level. For best rise and fall time of the video the comparators should be adjusted as close to the beginning of the desired video level as possible. An example is shown below.

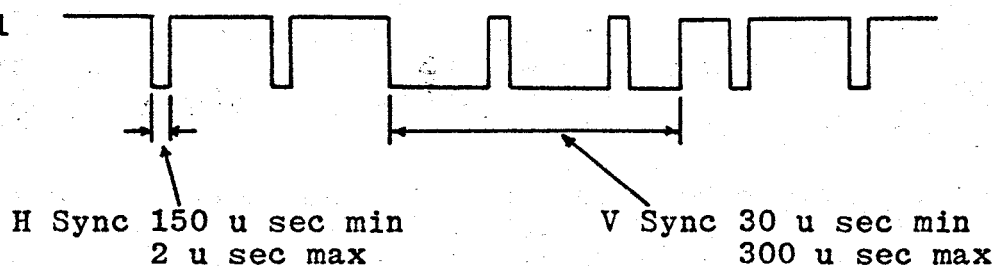


If the video is adjusted to Level A, the single dot characters and the double dot characters will appear the same intensity level. However, if the comparator were set to Level B, the double dot characters would be brighter than the single dot characters.

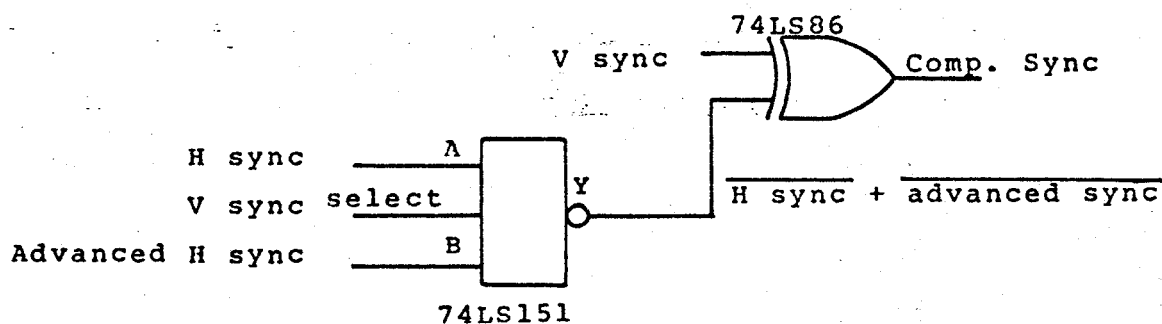
#### IV COMPOSITE VIDEO SYNC

The Sync should be provided as shown below

TTL High level  
2.0v to 5.2v  
TTL Low level  
0.0 to 0.8v



Note that the Horizontal Sync is advanced by the pulse width of the Horizontal Sync during Vertical Sync. This is done so the Phase Lock isn't out of lock at the end of Vertical Sync. The Phase Lock requires several scan lines to sync up once it is out of lock. A possible circuit is shown below.



## C. THEORY OF OPERATION

### I. Horizontal Section

IC 3 CD4046 is a phase lock loop (PLL) that drives the horizontal section. The internal oscillator frequency of the PLL is controlled by P2, R9, and C5. The sync input to the PLL is capacitively coupled from Pin G on the video board into Pin 14. The PLL syncs on the positive edge of the H sync pulse. The output of the PLL drives (Pin 4) the gate of the power MOS FET transistor, Q<sub>1</sub>.

The drain current of Q<sub>1</sub> is transformer coupled through T1 which provides the base drive for Q<sub>2</sub> (the horizontal output transistor). The horizontal retrace pulse from Q<sub>2</sub> is coupled through the voltage divider of R14 and R11 and is clamped to +12v by Zener diode D4.

This +12v pulse is brought back into the phase comparator of the PLL via Pin 3 of IC3. The output of the phase compactor is low pass filtered at Pin 13 of the PLL by the combination of R6, R10, and C17. The error voltage of the low pass filter is brought into Pin 9, the input to the PLL voltage controlled oscillator (VCO). The VCO sets the frequency of the PLL output (Pin 4). This horizontal drive is directly proportional to the input voltage.

The horizontal yoke has a saw tooth current that swings from +7 amps to -7 amps peak for 15" portrait models, and +9.5 amps to -9.5 amps for the Landscape models. Q<sub>2</sub> clamps the positive yoke voltage to the saturation voltage of the transistor during the positive yoke current. Catch diode D6 clamps the negative yoke voltage during the negative yoke current. When Q<sub>2</sub> is turned off the transition from + to - yoke current C23, 24, and 25 in combination with the horizontal yoke inductance sets the horizontal retrace time. The retrace time voltage wave form is half sine wave called the flyback pulse. The flyback pulse in combination with D5, T2 primary inductance, and C21, determines the boost voltage for the horizontal drive. The boost voltage sets the horizontal energy level and determines the horizontal width. The flyback pulse is stepped down through T2 to provide raw +10v and -10v. The +10v is regulated through IC4 which provides +6v for the CRT filament. The raw +10v and -10v are provided to the video boards via pins I and K respectively. The +10v is regulated on the video board to provide +5v for the TTL logic. The -10v is regulated to -5.2v for the ECL logic.



## Horizontal Section Continued

The horizontal yoke current goes through the linearity coil L1 through S caps C31 and C32 (which help control horizontal linearity) into the horizontal dynamic focus section where the S correction voltage is capacitively coupled through C33 into the primary of T3. The horizontal dynamic focus voltage is stepped up in the secondary of T 3 to approximately 300v and capacitively coupled into the focus grid through C 34 via blue wire 4.

The vertical dynamic focus is brought off C40 and capacitively coupled into the base of the transistor Q3. The collector of Q3 drives producing approximately 250v of vertical dynamic focus.

Power to the horizontal section is provided by the output of IC 1 which provides a maximum of 40v, adjusted by the horizontal width pot P1.

The high voltage power supply provides +1000v and -110v. The 1000v is divided to approximately 500v through P8 and R28 to drive the brightness grid on red wire 3. Also the brightness voltage can be controlled through the brightness transistor Q4, which is controlled by the op amp IC6 and the remote brightness pot. The 1000v is also divided by R27 and P7 to provide approximately 350v of focus voltage on blue wire 4. The -110v goes through D10, R11, and Zener D11 to control grid green wire 2, which is at about -57v at full contrast. The -110v has a "spot killer" circuit consisting of R31, C48, and D10, that holds a negative voltage on the control grid to avoid burning a spot in the CRT after AC power is removed. Power to the high voltage supply is provided by the output of regulator IC2 at approximately 25v.

## II VERTICAL SECTION

### VERTICAL DEFLECTION CIRCUIT

The heart of the vertical deflection circuit is IC5, the TDA 1170. The IC performs four major functions.

A Power Amplifier and Ramp Generator

Internal Oscillator

Voltage Doubler

Sync Input

The power amplifier provides the power to the vertical yoke from pin 4 of IC5. A current of 1 amp p-p is supplied to the vertical section of the yoke. The yoke current is capacitively coupled through C40 into the sense resistor R21. The sense resistor converts the yoke current into a 1v p-p voltage which is compared against the ramp out of pin 10, and includes the S correction for the vertical axis. This S correction is adjusted by the linearity correction pots P5 and P6.

The Internal Oscillator is set by the RC network R23, C43, and P3. It normally runs in the range from 45-63 Hz.

The input voltage of 25 volts on pin 2 from regulator IC1, is doubled to 50 volts in the doubling circuit D9, C36, and C35. The 50 volt output on pin 3 is used for the vertical flyback. Vertical sync input comes in on pin 8 from pin F on the video board connector which is driven by the LS14 on the video board. This vertical sync input IC4 clamps the sync voltage at .7 volts.

Power to the vertical section is provided by the output of IC2 which generates a voltage of approximately 25 volts.

### III TTL VIDEO BOARD THEORY OF OPERATION

The TTL video board has a video driver transistor Q1, collector supply voltage regulator IC1, and input buffer IC3, sync buffer IC4, and a +5v regulator (IC2) to drive IC3 & IC4.

The video driver transistor Q1 is a common emitter driver that swings between +30v and +1.8v. The +30v is produced by regulator IC1, TI 783CKC. The regulator is adjustable from 0v to +30v with the contrast Pot P1. This produces the same voltage swing on the cathode (collector of Q1) and also adjusts the control grid G1 from -91v to -61v.

Q1 is kept out of saturation (VCE +1.8v) by the combination of clamp diodes D3 & D4 & the VBE drop of Q1. Peaking inductor L1 speeds up the transistion time from +1.8v to +30v. IC3 (74S04) provides the base drive for Q1.

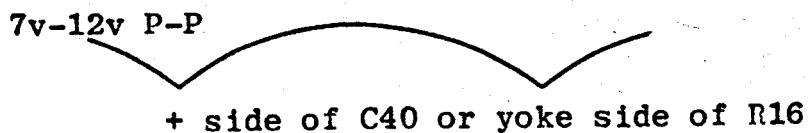
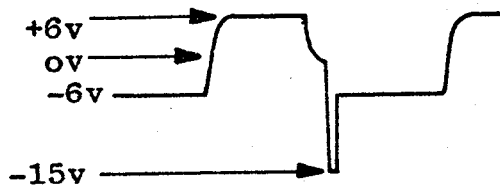
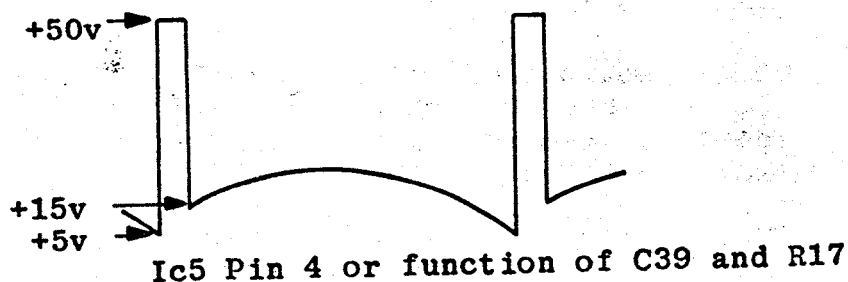
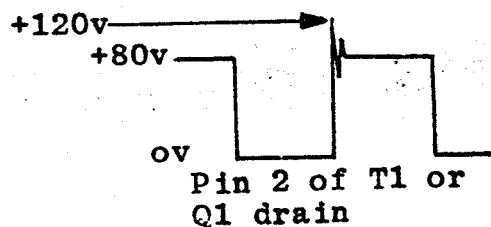
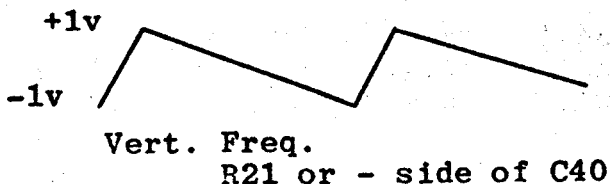
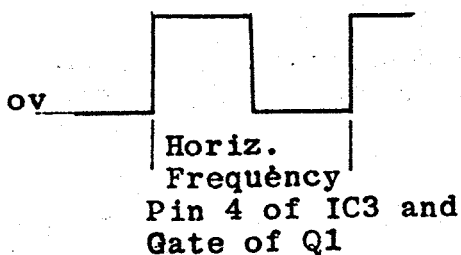
IC4 (74S14) inverts the horizontal and vertical sync inputs and drives the horizontal phase lock (CD4046) and the vertical deflection IC (TDA1170) on the deflection board. The TDA1170 clamps sync inputs to +.7v and R5 limits the current draw from IC4.

### IV ECL VIDEO THEORY OF OPERATION

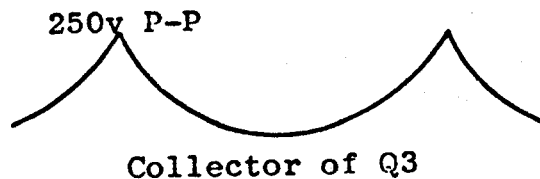
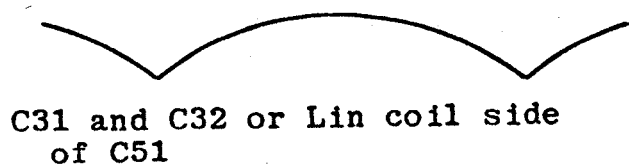
The ECL video board has a common base video transistor Q1 that drives the cathode and a second common base video transistor Q2 that is capacatively coupled into the control grid (G1). The emitter current of Q1 & Q2 is controlled by IC1 & IC2 (MC10115) defferential input ECL receivers. The emitter follower outputs of IC1 & IC2 are wire-ored, this keeps Q2 off when Q1 is on. Three discrete emitter current levels (60ma, 30ma, 15ma) can be switched into eight different combinations. This emitter current is translated into a voltage change by collector load resistors R4 & R7. As the cathode voltage (Q1 collector) goes from +25v to +9v the control grid voltage (D) goes from -82v to -67v. This collector voltage swing, produced by 100ma of current, gives a differential voltage swing of approximately 30v.

Also on the board are a series of 74LS14 inverters that are used to drive the horizontal and vertical sync inputs.

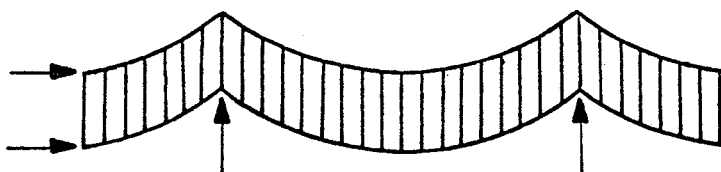
+15v



Pin 6 of T1 or Transformer  
side of R30, R42, R43



Horizontal  
Dynamic  
Focus  
Appr. 300v  
P-P

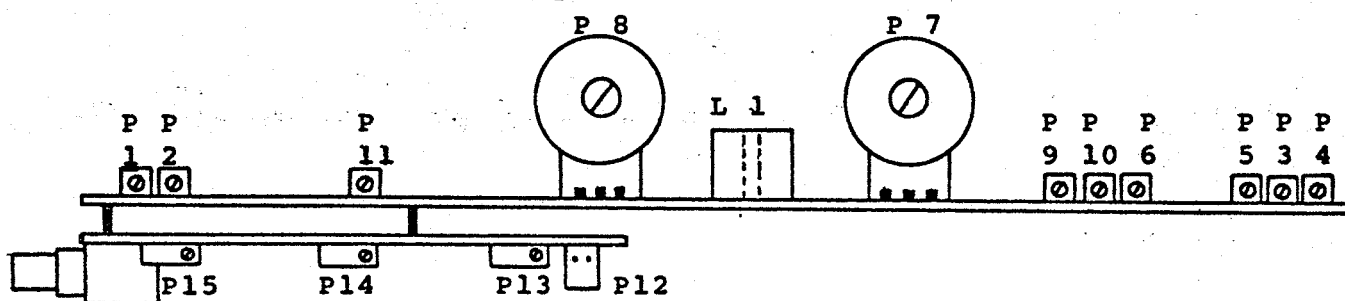


Vertical Dynamic  
Focus Appr. 250v P-P

The dynamic focus voltages vary somewhat from model to model.  
Wave form at the junction of C34 and R26.

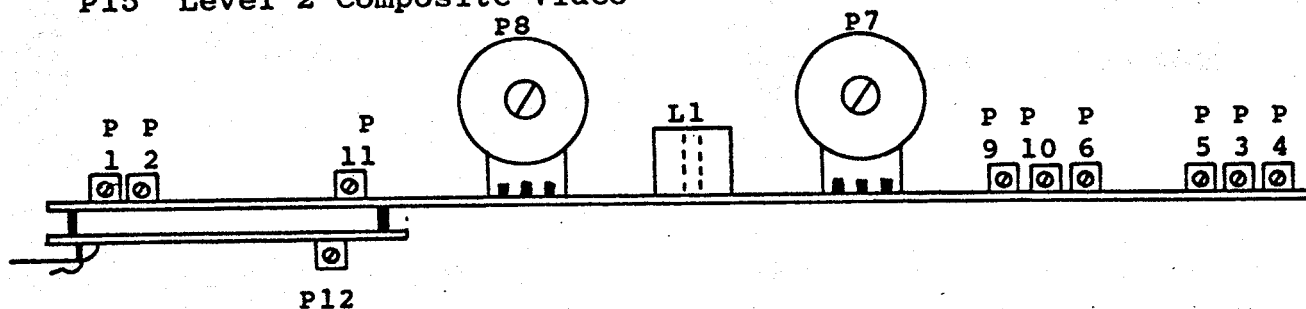
P1 Horizontal Width  
 P2 Horizontal Hold  
 P3 Vertical Hold  
 P4 Vertical Size  
 P5 Vertical Top Bottom Linearity  
 P6 Vertical Linearity  
 P7 D.C. Focus  
 P8 Brightness  
 P9 Vertical D.C. Centering  
 P10 Vertical Dynamic Focus  
 P11 Horizontal Dynamic Focus  
 P12 Video Contrast Connector  
 P13 Composite Sync Level  
 P14 Level 1 Composite Video  
 P15 Level 2 Composite Video

L1 Horizontal Linearity



P1 Horizontal Width  
 P2 Horizontal Hold  
 P3 Vertical Hold  
 P4 Vertical Size  
 P5 Vertical Top Bottom Linearity  
 P6 Vertical Linearity  
 P7 D.C. Focus  
 P8 Brightness  
 P9 Vertical D.C. Centering  
 P10 Vertical Dynamic Focus  
 P11 Horizontal Dynamic Focus  
 P12 Video Contrast Connector  
 P13 Composite Sync Level  
 P14 Level 1 Composite Video  
 P15 Level 2 Composite Video

L1 Horizontal Linearity



PART NO. 45526-30

CUSTOMER \_\_\_\_\_ SALES ORDER \_\_\_\_\_ TECH. \_\_\_\_\_

Unless otherwise specified:  $V_{cc} = (nom)$ ,  $I_{O} = 1/2 I_{O} (max.)$ ,  $T_a = 25^{\circ} \pm 5^{\circ}C$ .

Input Lines,  $V_{in}$ : Min 103  $V_{RMS}$ , NOM 115  $V_{RMS}$ , MAX 130  $V_{RMS}$ , TRANS 140  $V_{RMS}$

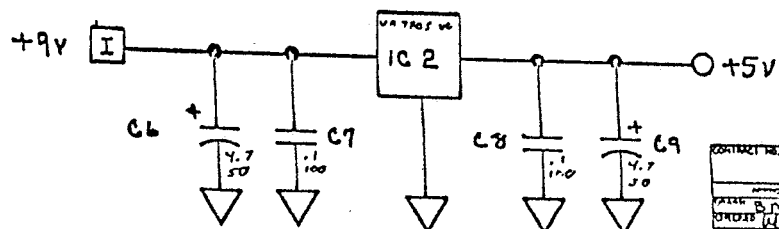
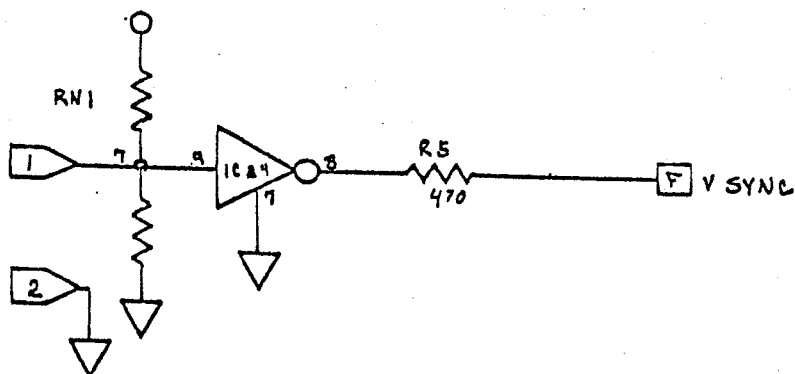
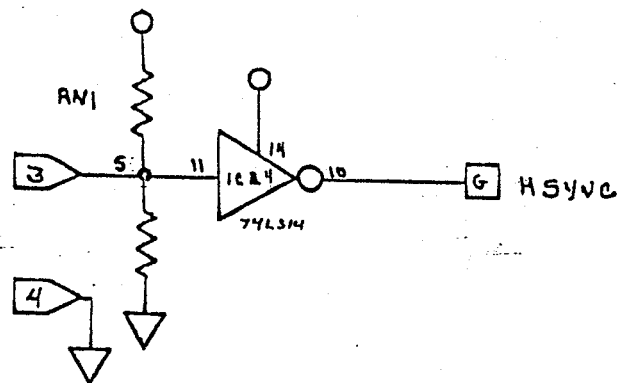
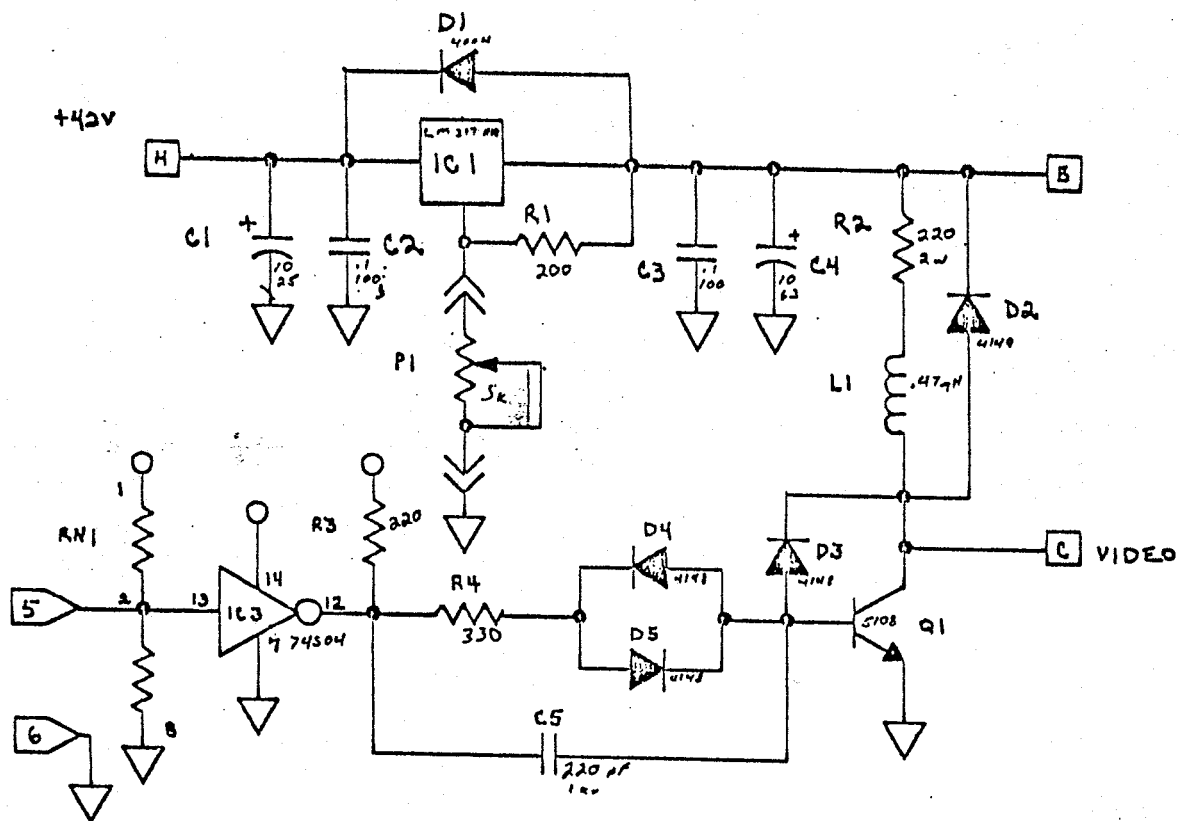
HI POT TEST 1700/sec VDC INPUT TO CHASSIS. INPUT TO OUTPUT, 100 VDC 10 MEGRMIN. OUTPUT TO CHASSIS & O/P TO O/P. IF APPL.

Rev.	Drawn	App'd	Date
—	MD	201	10/1/2

[illegible]

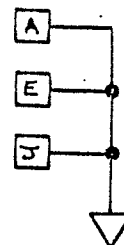






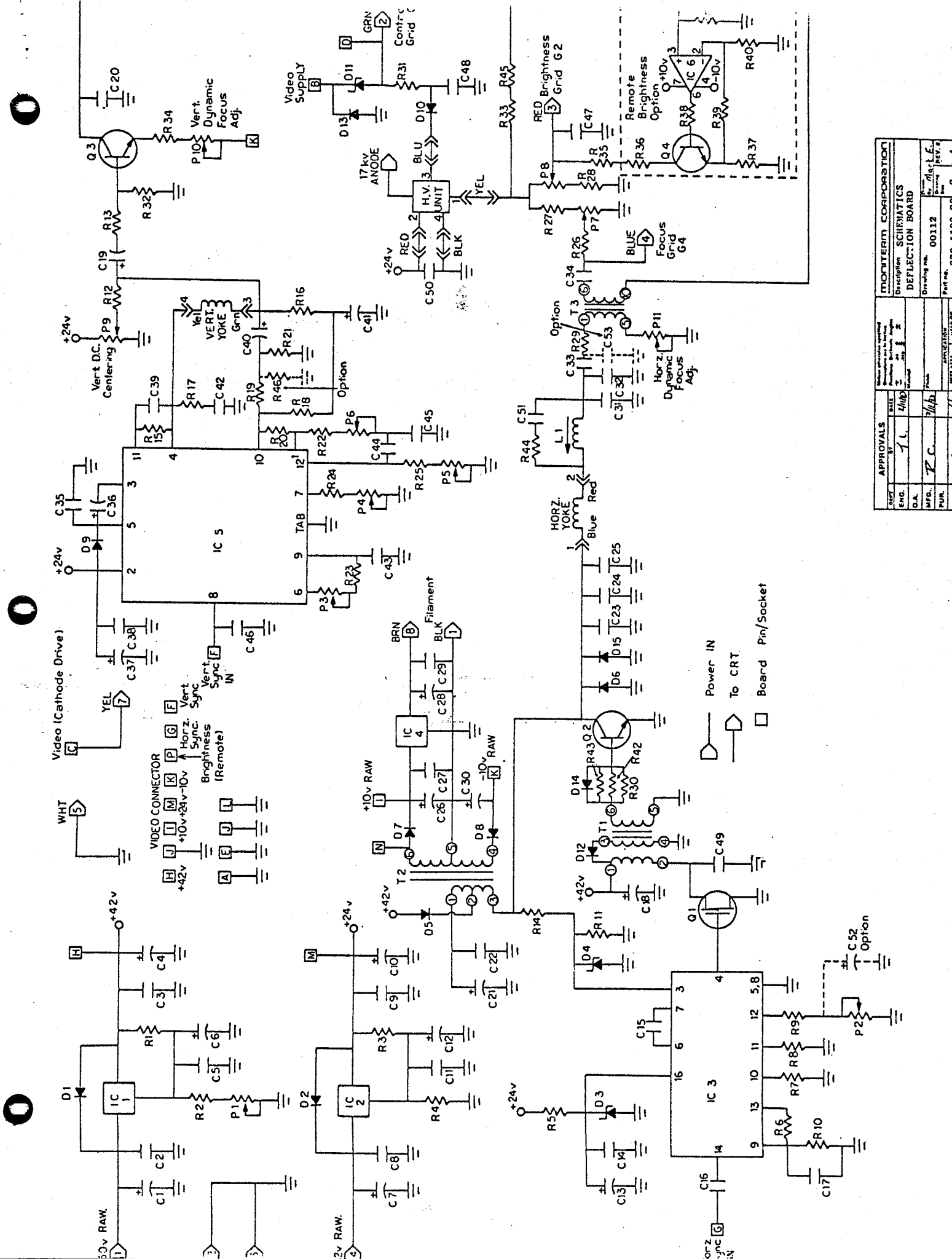
+42V [H]

-9V [K]



CONTRACT NO.		MCKINSTRON CORPORATION	
DATE	REV	DATE	REV
3/1/82	1	3/1/82	1
TTL BOARD		80050	





APPROVALS		MONITOR CORPORATION	
DESIGNED BY	DATE	DESCRIPTION	SCHEMATICS
ENG.	1/1	DEFLECTION BOARD	
APP.	1/1	DRAWING NO.	00112
PUR.	1/1	PART NO.	670-1100-00
P.A.	1/1	SCALE	2-1
		SHEET	1 OF 1

