UM607

DIGIVUE®
USER MANUAL
512-60

DISPLAY D141

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DISPLAY D141

Owens-Illinois, Inc.
Electro/Optical Display Business Operations
Post Office Box 1035
Toledo, Ohio 43666
(419) 242-6543

Owens-Illinois, International S.A.
50, route des Acacias
1227 Carouge-Geneva, Switzerland
(022) 43 62 00

OWENS-ILLINOIS

$5.00

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DIGIVUE® display/memory units are designed and produced for OEM (Original Equipment Manufacturer) applications, and as such are intended to be mounted in the purchaser's equipment or product. It is the responsibility of the purchaser to insure, as necessary, that the display unit and power pack are installed and used in accordance with Underwriter's Laboratories, government, or other applicable rules and regulations governing their end use (such as UL 114, NFPA pamphlet 75). Certain items which may be supplied with the display unit or power pack (e.g., cover, power switch, AC cord, etc.) are for the convenience of the purchaser only and are not intended to suggest possible uses for the display unit or power pack. Nor do they indicate that the display unit or power pack may be used as an end product as received by the purchaser without being incorporated into his equipment or in some way modified to meet the appropriate rules and regulations governing the end use of the display system.

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ILLUSTRATIONS

1.0 INTRODUCTION

This manual provides general information useful to the system designer and display user for the proper installation and operation of the 512-60 DIGIVUE® display/memory unit, model D141.

The 512-60 DIGIVUE® display/memory unit is a digitally addressed alphanumeric/graphic display which uses a 512 line by 512 line gas discharge panel as its display medium. Information is displayed in dot matrix form by selectively established light producing gas discharges. These discharges may be randomly turned on or off (WRITTEN or ERASED) without disturbing any other information already present in the display, or they may all be turned off (BULK ERASED) in one operation.

Once information has been displayed it will remain without any external influence so long as power to the display is not interrupted. This ability to maintain information is referred to as INHERENT MEMORY.

The display requires no refreshing; it is only necessary to store addresses pertinent to the displayed information as needed to process data (information may not be retrieved electronically from the display unit).

2.0 GENERAL

2.1 Typical Characteristics

Physical:	
Dot matrix size	512 x 512
Resolution	60 Dots per inch (24 dots per cm)
Dot spacing	16.7 mils (.42mm) center to center
Display size (active area)	8.5" x 8.5" (21.7 cm x 21.7 cm)
Character capacity:[1]	
5 x 7 (6 x 10) Matrix	4335 Characters 51 Lines 85 Characters per line
7 x 9 (8 x 16) Matrix	2048 Characters 32 Lines 64 Characters per line
Dot brightness	60 footlamberts
Contrast ratio	15:1
Dot size	9 mils (.23 mm)
Viewing angle	160°
Color	Neon orange (5852 Å predominant)
Electrical:	
Data interface:	
Input	9 X Address lines 9 Y Address lines 2 Control lines (select WRITE, ERASE, and BULK ERASE operations)
Output	SYNC (50KHz clock) STATUS (Busy/Done indicator)
Type interface	TTL with resistor pull up to V_{CC}
Operational rates:	
Maximum address rate	50K dots per second
Character rate	833 characters per second [5x7 (6x10) Matrix] 390 characters per second [7x9 (8x16) Matrix]
Full panel bulk erase	20 microseconds
Automatic bulk erase	30 minutes after last address operation
Data modes	Asynchronous or synchronous
Mechanical:	
Size	See figure 2.1
Weight	34 pounds (15.4 Kg)
Environmental:	
Temperature range:	
Operational	0°C to +50°C (0°C to +35°C)[2]
Storage	-40°C to +70°C (-40°C to +50°C)[2]
Humidity	10-80% noncondensing/noncorrosive[3]

1-Display is non-formatted, character matrix sizes are given for information only.

2-Parenthesized ranges refer to display with contrast enhancing filter and rear projection screen installed.

3-Without contrast enhancing filter and rear projection screen installed.

2.2 Dimensions

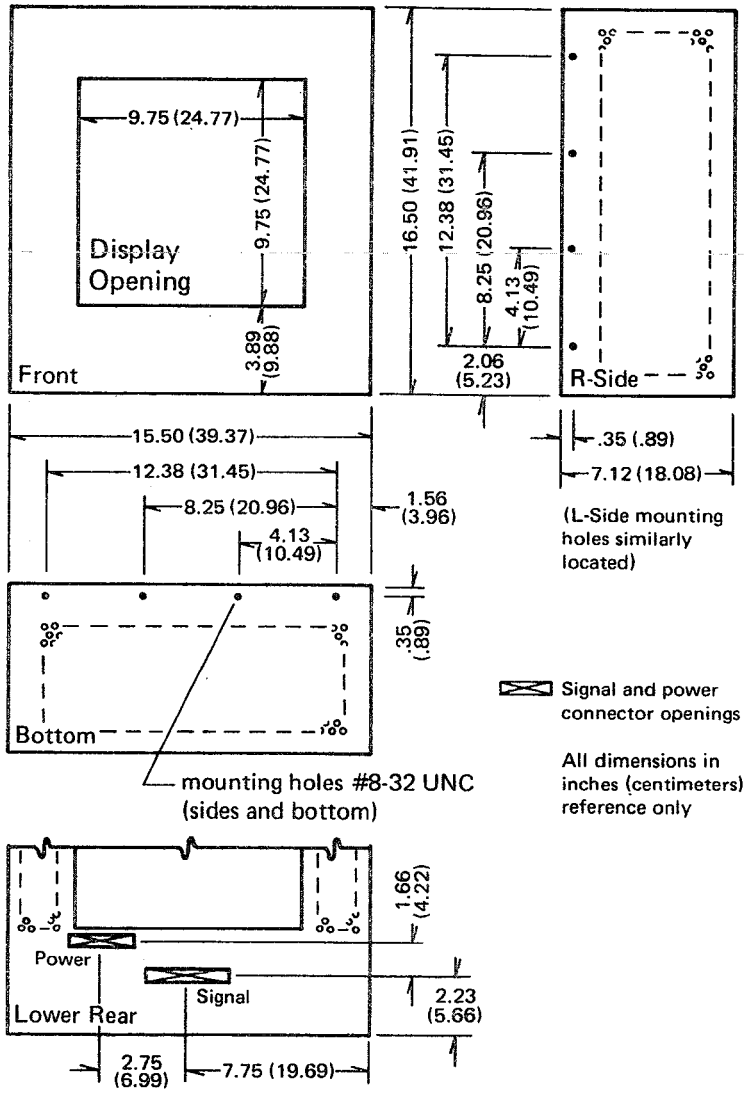

Figure 2.1 - Display Dimensions

2.3 Rear Projection

This display has several unique characteristics which allow the projection of images onto the rear of the display panel. In this way, photographic images of forms, maps, or any other projectable material may be integrated with displayed information.

A frosted projection screen is provided on the rear surface of the display panel. Figure 2.2 illustrates its position in relation to the plane of the gas discharges in the display. When using the rear projection capability, consideration should be given to the parallax resulting from the separation of the planes of the gas discharge and the projected image.

If the rear projection capability is not to be used, it is suggested that a piece of black paper be placed over the rear of the projection screen to shut out ambient light and insure maximum display contrast.

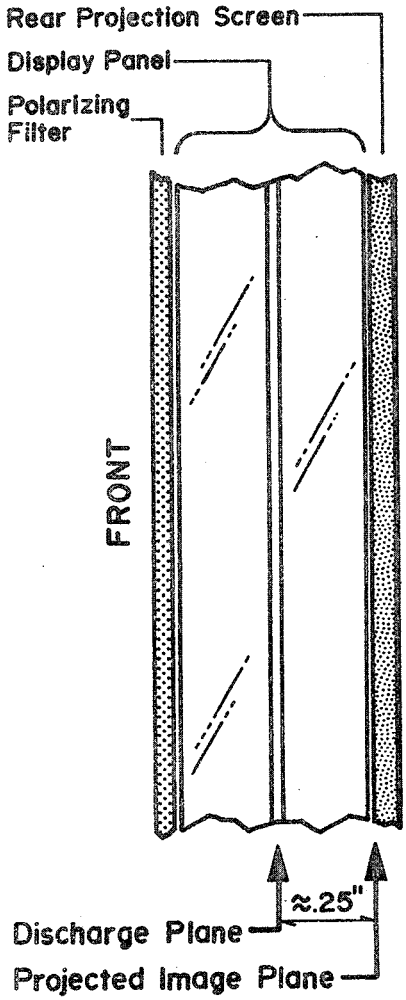

Figure 2.2 - Cross Sectional View of Panel Assembly

2.4 Display Origin

The display origin (0,0 coordinate) is located in the lower left corner of the display matrix. It can, if necessary, be relocated to the upper left corner. Contact our Field Service department for further information [(419) 242-6543, ext. 66-468].

2.5 Cleaning

Avoid allowing any object, particularly fingers, to contact the surface of the polarizing filter and rear projection screen installed on the display panel. These surfaces can be permanently marred and their usefulness impaired through careless use or improper cleaning.

To clean the polarizing filter and rear projection screen, first remove loose soil by lightly dusting them with a soft cloth or tissue. Then, using only a mild detergent and water solution on a soft cloth or tissue, gently wipe the surface until it is clean. If the surface is soiled by a dried or gritty material, carefully moisten the soiled area until the material is dissolved or loosened before wiping it away. Dry the surface with

a soft cloth or tissue. Never scrub the surface or use cleaning solvents.

The display enclosure may be cleaned using a soft cloth moistened with a mild detergent and water solution. Wring the cloth well to avoid getting the cleaning solution inside the enclosure.

3.0 INTERFACE SIGNALS

3.1 Interface Signal Levels and Conventions

The positive logic convention is used to describe interface signal levels for the display. HI indicates the more positive voltage level; the logical "1" or "true" state. LO indicates the more negative voltage level (at or near system ground); the logical "0" or "false" state.

The following signal voltage specifications are as measured at the interface connector on the display unit:

LO input	=	+0.8 VDC maximum
HI input	=	+2.0 VDC minimum
LO output	=	+0.8 VDC maximum
HI output	=	+2.4 VDC minimum

Each interface input signal is terminated inside the display by a 1000 ohm resistor to +5 VDC (Vcc) and buffered by a 7400 series TTL logic element.

Each interface output signal as it appears at the interface connector either represents or is capable of driving one standard TTL unit load.

3.2 Address Signal Inputs

The selection of the individual gas discharge sites or LIGHT POINTS to be written or erased in the display matrix is accomplished through 18 address input signals.

These signals are divided into 2 nine bit words; one word specifying the coordinate of the selected point in the X (horizontal) axis, and the other in the Y (vertical) axis. The bits in each word are numbered 0 through 8; i.e., X_0, $X_1 \ldots X_8$ and Y_0, $Y_1 \ldots Y_8$, and have binary values of 1 through 256 respectively. The X and Y point coordinates may, therefore, be assigned any value from 0 through 511.

If all ADDRESS signals are LO, the point selected will be located at the display origin (0,0 coordinate location).

3.3 Control Signal Inputs

The display WRITES or ERASES individually addressed points in the display matrix, or BULK ERASES all illuminated points simultaneously, as directed by two control input signals, C_0 and C_1. The use of these signals is illustrated in figure 3.1.

As a convenience in existing applications where earlier model 512-60 displays have been used, individual WRITE, ERASE, and BULK ERASE control signals have been provided. These signals serve the same function as the C_0 and C_1 signals and are used as illustrated in figure 3.2.

Either set of control signals may be used, but not simultaneously.

CONTROL SIGNALS C_0	C_1	DISPLAY OPERATION
1	1	Idle
1	0	Write
0	1	Erase
0	0	Bulk Erase

Figure 3.1 - Control Signals and Display Operation

CONTROL SIGNALS *WRITE*	*ERASE*	*BULK*	DISPLAY OPERATION
0	0	0	Idle
1	0	0	Write
0	1	0	Erase
0	1	1	Bulk Erase

Figure 3.2 - Alternate Control Signals and Display Operation

3.4 STATUS Signal Output

STATUS is an output signal which serves as the display busy/done indicator.

When the display is idle, with or without information being displayed, STATUS will rest in the HI state. STATUS goes LO to indicate that the display is busy executing operations as directed by the CONTROL signals.

3.5 SYNC Signal Output

SYNC is a display generated clock output which is used to synchronize external circuits with the operation of the display. SYNC is normally LO with a positive going pulse occurring every 20 microseconds (50KHz).

3.6 Interface Signal Connector

All logic level interface signals associated with display operation are accessible through the printed circuit edge connector on the rear of the display enclosure. Figure 3.3 lists the pin assignments for this connector.

PIN #	SIGNAL	PIN #	SIGNAL
1	Gnd*	16	N/C
2	+5VDC*	17	Y1
3	SYNC	18	X1
4	STATUS	19	X2
5	Write	20	X4
6	Bulk †	21	Y8
7	Erase	22	Y3
8	X0	23	Y4
9	X3	24	Y6
10	X5	25	Y7
11	X7	26	Y2
12	X6	27	Y5
13	X8	28	Y0
14	C_0	29	Chassis Gnd
15	C_1	30	Signal Gnd

Pins A through j - Signal Gnd

**Voltage output - 375ma (max) (see section 5.3)*

†*Key*

Figure 3.3 - Interface Connector Wiring List

Mating Connector Type:

Manufacturer: AMP

Part	QTY	Mfg. Part No.
Housing	1	1-583718-3
Contacts	60	583854-5
Key	1	583274-1

4.0 DISPLAY OPERATION

4.1 Asynchronous Mode

The display may be addressed asynchronously by presenting the appropriate ADDRESS and CONTROL signals simultaneously while STATUS is resting in the HI state (see figure 4.1). Within 20 microseconds after presentation of these signals, STATUS will go LO indicating that the display has begun execution of the requested operation.

The CONTROL SIGNALS may be returned to their idle state or be updated for the next operation after the HI to LO transition or STATUS.

The ADDRESS SIGNALS are not stored by the display so they must be held at their appropriate level the entire time that STATUS is LO. After the display has completed execution of the requested operation and STATUS has returned HI, the ADDRESS SIGNALS may be changed.

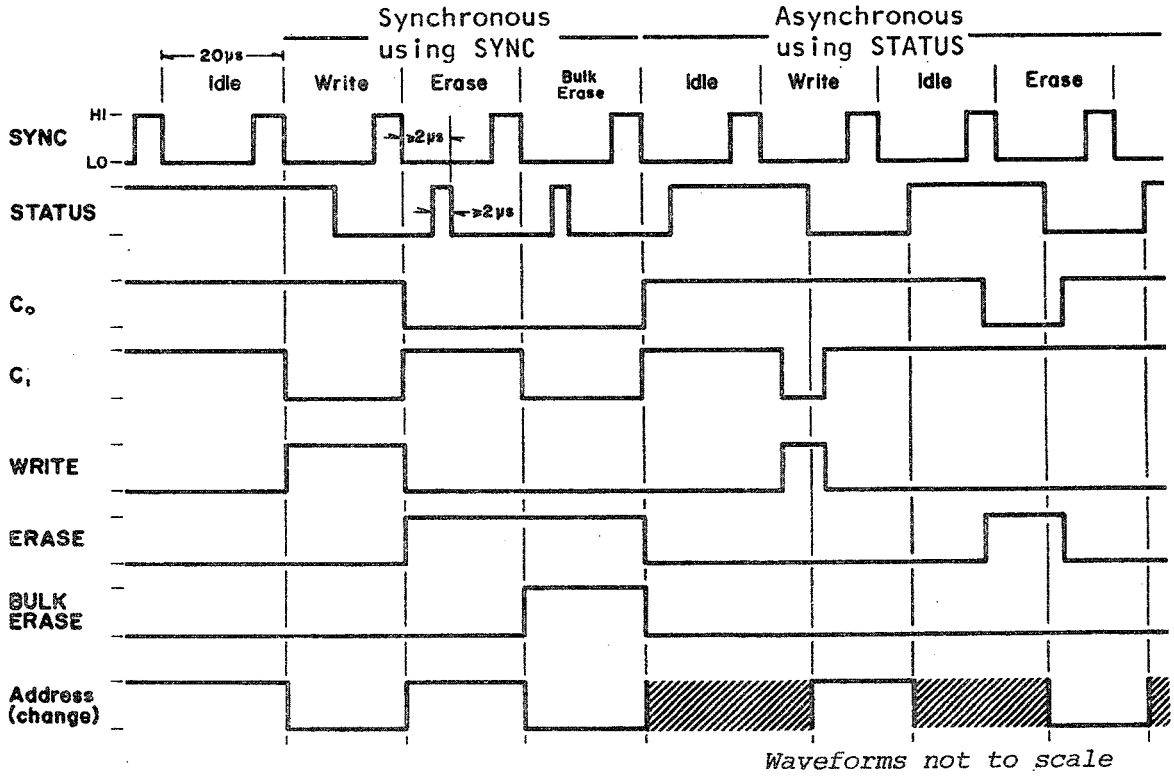

Figure 4.1 - Typical Interface Signal Waveforms

If another operation has been requested by the CONTROL SIGNALS as STATUS returns HI, STATUS will remain HI for a minimum of 2 microseconds before once again going LO, to indicate that the display has begun execution of the new operation. The ADDRESS SIGNALS must be updated for the new operation while STATUS is HI.

4.2 Synchronous Mode

The display may be addressed synchronously at its maximum address rate by using the SYNC signal. This is accomplished by presenting and then subsequently updating the appropriate ADDRESS and CONTROL signals within 2 microseconds following the HI to LO transition of the SYNC signal (see figure 4.1). The ADDRESS and CONTROL signals should not change until the reoccurrence of the SYNC signal HI to LO transition.

For added flexibility, the display may be addressed synchronously using the SYNC and STATUS signals. In this case, the ADDRESS and CONTROL signals are presented or updated within 2 microseconds following the HI to LO transition of the SYNC signal as described in the foregoing paragraph. However, if desired, the CONTROL signals may be changed as soon as STATUS goes LO. The ADDRESS signals must remain at their appropriate levels until the reoccurrence of the SYNC signal's HI to LO transition.

4.3 Automatic Bulk Erase

Automatic bulk erase is a display controlled operation which automatically erases the entire display screen when the display has been left idle for an extended period of time. The automatic bulk erase will be executed approximately 30 minutes after the last operation regardless of whether information is actually being displayed, and will repeat at 30 minute intervals for as long as the display is turned on and left idle.

CAUTION

Automatic bulk erase is provided to protect the display and extend its life. Do not leave the display idle with the CONTROL signals set for a WRITE or ERASE operation as this will disable the AUTOMATIC BULK ERASE feature. (See section 4.4, Uniform Display Usage.)

4.4 Uniform Display Usage

As the display is used, the operational characteristics of each discharge site change slightly dependent upon the accumulated time that the discharge site has been illuminated. Such changes that may occur during the life of the display after the display has been in service for an extended period of time can be easily compensated for through minor voltage readjustments.

When varied types and formats of information are displayed evenly throughout the display area, all of the discharge sites are used rather uniformly and maximum display life can be expected. If, however, it is necessary to repeatedly display fixed format information (i.e., cursor home positions, headings, redundant messages), particularly if such information is to be displayed for extended periods of time, the life of the display can be enhanced by observing the following practices. When possible, continually displaying the same fixed format material should be avoided. When such material is displayed, it should be bulk erased as soon as possible after it has been used. A better practice is to call up fixed format material for only as long and as often as required. If fixed format material must be displayed continually, its position should be shifted periodically to different areas of the display. Any convenient method of message shifting can be used but it should involve as large an area of the display panel and as many of the discharge sites within that area as possible.

4.5 Display Duty Cycle

The display can be operated continuously with up to 50% of the light points turned on.

With 100% of the light points turned on, the display should not be operated for a period of time exceeding five minutes.

If the S159 power pack is used to power the display and the display is operated at 100% capacity for longer than 5 minutes, power pack fuse F4 will open to protect the display system. (Refer to user manual UM609 for power pack fuse locations and replacement procedure.)

5.0 POWER INPUT REQUIREMENTS

5.1 Power Supply Requirements

The following voltages are required for display operation:

DC Voltage[1]	Amperes (Max)	Total Regulation
+5 (V_{CC})[2]	3.75	1%
+9 (V_{SC})	2.0	30%
+65 to +85 (V_{AX})[3]	.175	.5%
-65 to -85 (V_{AY})[3]	.175	.5%
+80 to +100 (V_{SS})	.7	.5%
+38 (V_{SB})[4]	.05	10%

1-Measured at display power input connector
2-Remote sense lines are provided
3-Supply output must have less than 1000pf capacitance to ground
4-For approximately 20 seconds after power is first applied, V_{SB} must boost to +125VDC.

The S159 model 512-60 DIGIVUE display.memory unit power pack has been designed to provide all voltages necessary for the operation of the D141 display. If this supply is to be used with the display, refer to User Manual UM609 for instructions regarding its operation.

5.2 Power Input Connections

Figure 5.1 illustrates the power supply connections to the display. The cable between the power supplies and display should be as short as possible (5 feet maximum is recommended) and it should be fabricated from 18 AWG wire minimum.

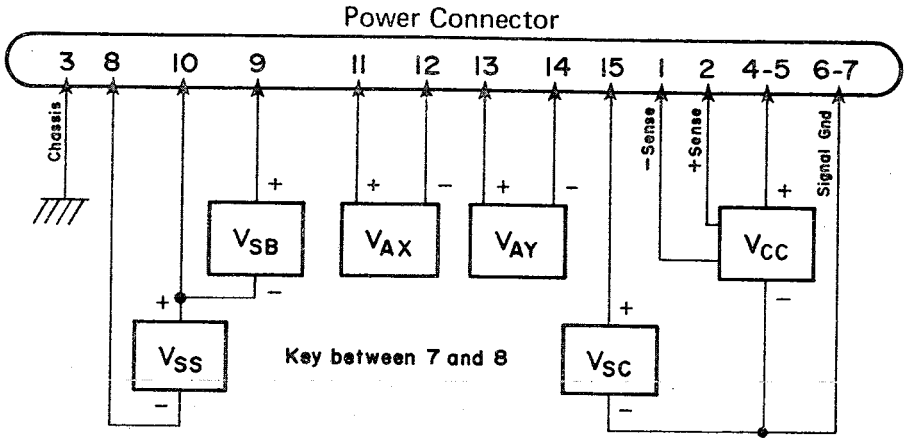

Figure 5.1 - Power Supply Connection Diagram

CAUTION

NEVER make or break the connection between DC power source and the display without first removing all power from the system.

Mating Connector Type:

Manufacturer: AMP

Part	Qty.	Mfg. Part No.
Housing	1	583301-1
Contacts	15	583362-4
Key	1	583462-1

5.3 5VDC Output

5VDC from the power input connector is available on pin 2 of the interface signal connector and may be used to power a small interface, test, or other circuit requiring less than 375 milliamperes of current.

The fuse for the 5VDC output is mounted inside the display enclosure. Refer to the D141 display maintenance manual UM608 for fuse replacement procedure.

6.0 INSTALLATION

6.1 Ventilation

The display is designed to be adequately cooled by convection air movement as long as the environmental requirements of the display are met and the display is mounted in accordance with section 6.2. As with all electronic equipment, the life and performance of the display can be enhanced by providing some form of forced air cooling.

CAUTION

The display is rated for use in a temperature range of 0°C to +50°C. However, the contrast enhancing filter and rear projection screen supplied with the display are rated for use in a range of 0°C to +35°C.

6.2 Mounting

The display should be mounted in its normal upright position (arrow on side of cabinet pointing upward) to allow proper convection air cooling of the unit. If adequate forced air cooling is provided, the display may be mounted in any position.

The display should be installed away from heat sources such as radiators or equipment hot air exhausts. Ventilation holes in the cabinet must remain unobstructed to allow proper convection air cooling of the display electronics. If any of the ventilation holes are covered in installation, forced air cooling must be provided.

Threaded holes are provided in the display cabinet for mounting. The locations and size of these holes are indicated in figure 2.1.

7.0 POWER APPLICATION AND ADJUSTMENTS

7.1 Initial Power Application

Before applying power to the display, check to insure that all power and signal connections are properly and securely assembled.

7.1.1 Using the S159 Power Pack

WARNING

Before connecting the power pack to the AC source, check to insure that it has been wired for the appropriate AC input voltage. (Refer to the S159 power pack user manual UM609 for instructions for changing the power pack AC input voltage range.)

If the S159 power pack is being used with the display, merely apply AC power to the power pack. With 30 seconds the glow of the preconditioning discharges should be visible around the perimeter of the display panel. (It is normal for the glow to be bright initially and then dim.) If this glow does not become apparent within the specified time, turn off AC power, wait approximately 10 seconds, reapply AC power, and check for the glow again. If the glow still does not appear, turn off AC power and check the following:

1) All connections to insure proper assembly

2) AC power source

3) Display panel for breakage

4) Fuses in the power pack

This initial turn on sequence is intended to quickly check for proper system setup. Once proper operation has been initially verified, the display may be addressed 200 milliseconds after AC power is subsequently applied.

7.1.2 Using Laboratory Supplies

When supplying power to the display from individual power supplies, the following procedure should be used.

CAUTION

Turn on power supplies in the prescribed sequence. Failure to do so may result in damage to the display.

Note: All voltages to be measured at the power input connector

1) Turn on the V_{CC} supply and adjust to 5VDC.

2) Turn on V_{SC} supply and adjust to 9VDC.

3) Insure that V_{CC} and V_{SC} supplies have reached their full output, then turn on the V_{AX} and V_{AY} supplies and adjust them to the voltage indicated on the blue system information card supplied with the display.

4) Turn on the V_{SS} supply and adjust it to the voltage indicated on the blue system information card supplied with the display. (If the display does not work properly at this setting, see Section 7.2 for V_{SS} readjustment procedure.)

5) Turn on the V_{SB} supply and increase its output to at least 100VDC (130VDC maximum) until the preconditioning discharges are established around the perimeter of the display panel. When the discharges have been established, reduce V_{SB} to its normal operating level of approximately 40VDC.

If individual power supplies are to be automatically sequenced on, they may be turned on in groups as follows (output voltages may be preset):

1) Turn on V_{CC} and V_{SC} simultaneously

2) AFTER V_{CC} and V_{SC} supplies have reached full output, turn on remainder of

supplies. (V_{SB} should be 130VDC for approximately 20 seconds after power is first turned on; then drop to a normal operation level of 40VDC. The display is normally ready to be addressed 200 milliseconds after V_{SS} and V_{SB} have been applied.)

To remove power from the display, the power supplies should be turned off in the following order:

WARNING

NEVER remove power from the display by disconnecting the power input connector.

1) V_{SB}

2) V_{SS}

3) V_{AX} and V_{AY}

4) V_{SC} and V_{CC}

7.2 Voltage Adjustments

When the S159 power pack is used to provide power to the display, adjustment of individual voltages is not necessary since the power pack shipped with the display has been preadjusted for proper display operation. However, after the display has been used for an extended period of time, the power pack voltages may require adjustment. The need for voltage readjustment is generally indicated by incomplete writing or erasing of information in the display, or by the appearance of unwanted light points while performing a writing operation. Refer to user manual UM609 for power pack voltage readjustment procedures.

When power is supplied to the display by some source other than the S159 power pack, proper display operation should result when the power supply voltage levels are

adjusted as described in section 7.1 of this manual. If that procedure does not result in proper display operation, proceed as follows:

When adjusting voltages, it will be necessary to scan a pattern on the display so that approximately 25% of the light points are written. The pattern can be a specially generated one for voltage adjustments, or it can be a page of text or any other available material.

1) Adjust the power supplies as follows:

V_{CC}	5V
V_{SC}	9V
V_{SS},V_{AX},V_{AY}	Adjust to voltage levels indicated on blue system information card supplied with the display.
V_{SB}	Increase until the preconditioning discharges are established around the perimeter of the display panel (130V maximum); then, decrease to approximately 40V.

2) Scan the display with the test pattern and check for proper operation. If possible, selectively erase the test pattern and check for its complete erasure.

3) If some points fail to write when the pattern is scanned onto the display, V_{SS} is probably low. Slowly increase V_{SS} while repeatedly writing and erasing the test pattern (selective erase is preferable, but bulk erase may be used if necessary). Increase V_{SS} until the display writes properly, then increase it one additional volt and record its final setting for reference. (Adjustment complete)

4) If some points are being written that are not addressed, V_{SS} is probably too high. Decrease V_{SS} to approximately 85V, then slowly increase it using the procedure in step 3, above.

If there is any difficulty in adjusting voltages, contact our field service department at (419) 242-6543, ext. 66-217.

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POWER PACK
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Owens-Illinois, Inc.
Electro/Optical Display Business Operations
Post Office Box 1035
Toledo, Ohio 43666
(419) 242-6543

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50, route des Acacias
1227 Carouge-Geneva, Switzerland
(022) 43 62 00

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CONTENTS

ILLUSTRATIONS

1.0 INTRODUCTION

This manual contains information for the proper installation and operation of the DIGIVUE® display/memory power packs, S159 and S205.

The S159 and S205 power packs are multiple output power sources designed specifically for use with certain models of DIGIVUE® display/memory units. Both power packs are functionally identical, the only difference being the S205 does not include a cover or AC power switch. Both power packs are compact, easily installed, and provide all voltages necessary for the efficient operation of the display for which they were designed.

Before attempting to use either of these power packs, consult the appropriate display user's manual to verify display/power pack compatibility.

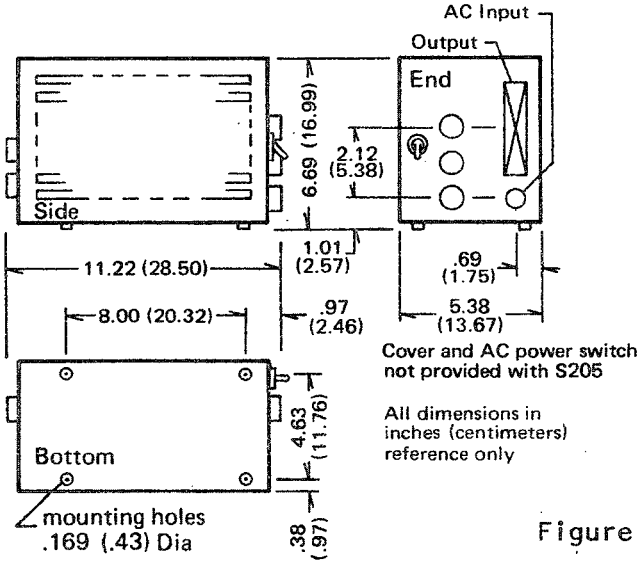
2.0 GENERAL

2.1 Typical Characteristics

Mechanical:	
Size	See figure 2.1 and drawing CP340M1200
Weight	23.5 pounds (10.5 Kg)
Environmental:	
Temperature range:	
Operational	0°C to +50°C
Storage	-40°C to +70°C
Humidity	10-80% noncondensing/noncorrosive
Power:	
Input	105-125 VAC 50/60Hz 2.5 amperes 210-240 VAC 50/60Hz 1.25 amperes

Output

DC Voltages		Amperes (max)	Total Regulation[1]
V_{CC}[2]	+4.8 to +5.25	3.75	.7%
V_{SC}[5]	+9 ±1	2.0	30%
V_{AX}	+65 to +85	.175	.5%
V_{AY}	-65 to -85	.175	.5%
V_{SS}	+85 to +105	.7[3]	.5%
V_{SB}[4,5]	+38 ±10	.050	10%



1-Includes the effects of line, load, and temperature variations.
2-Remote sensing provided.
3-For intermittent periods of less than 5 minutes.
4-For approximately 20 seconds after AC power is first applied, V_{SB} boosts to a level within a range of +100 to +130 volts DC.
5-Nonadjustable.

Figure 2.1 - Mechanical Dimensions

2.2 Protection

The power pack is protected against overcurrent conditions by the following means:

Input: 105-125VAC 4A Slo-Blo line fuse
210-240VAC 2A Slo-Blo line fuse

Output:

Supply	Type
V_{CC}	5A Fuse/Current limiting
V_{SC}	3A Fuse
V_{AX}	.25A Fuse/Current limiting
V_{AY}	.25A Fuse/Current limiting
V_{SS}	.6A Fuse/Current limiting
V_{SB}	.375A and .6A (boost circuit) fuses

Power transformer thermal cutout (automatic reset)

2.3 Power Pack and Display Pairing

A power pack which accompanies a display unit in shipment has been preadjusted for the proper operation of that display. (The serial numbers of the paired display and power pack are noted on the system information card attached to the display.) The power pack can be used with any other compatible display; however, it may be necessary to readjust the V_{SS}, V_{AX}, or V_{AY} voltage level (see section 4.2 for procedure).

2.4 Power Output Connector

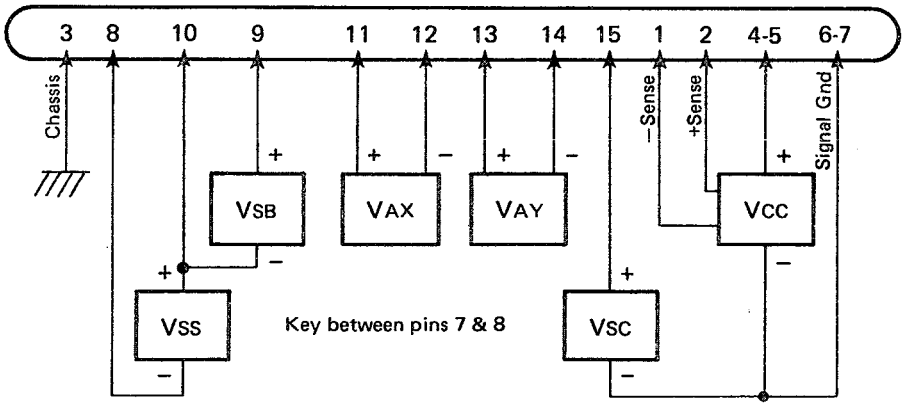


Figure 2.2 - Power Output Connector

Mating connector type:

Manufacturer — AMP

Part	Qty	MFG. Part No.
Housing	1	583301-1
Contacts	15	583362-4
Key	1	583462-1

3.0 INSTALLATION

3.1 Ventilation

The power pack is designed to be adequately cooled by convection air movement as long as the environmental requirements of the power pack are met and the power pack is mounted in accordance with section 3.2. As with all electronic equipment, the life and performance of the power pack can be enhanced by providing some form of forced air cooling.

3.2 Mounting

The power pack should be mounted in its normal upright position (arrow on side of chassis pointing upward) to allow proper convection air cooling of the unit. If adequate forced air cooling is provided, the power pack may be mounted in any position.

The power pack should be installed away from heat sources such as radiators or equipment hot air exhausts. Ventilation holes in the cover (if a cover is provided) must remain unobstructed to allow proper convection air cooling of the power pack circuitry. If any of the ventilation holes are covered in installation, forced air cooling must be provided.

Mounting holes are provided on the bottom of the power pack chassis. The locations and size of these holes are indicated in drawing CP340M1200 (provided in the back of this manual).

3.3 Connecting to the Display

CAUTION

Do not connect the power pack to the display while AC power is applied. To do so may damage the display. Refer to the appropriate display user manual for initial power application instructions.

The power pack is connected to the display using the power interconnect cable. (The cable is shipped assembled to the power input connector of the display.)

Remove the two 4-40 screws at the ends of the power pack output connector and connect the power interconnect cable. The cable connector is keyed for proper assembly to the power pack. Using

the two 4-40 screws previously removed, secure the power interconnect cable to the power pack.

3.4 Power Interconnect Cable Length

The power interconnect cable supplied with the power pack can be lengthened, or a new one made, using UL style 1007-18 AWG (minimum) wire. The cable length should not exceed 5 feet (1.5 meter).

3.5 AC Input and Power Range

The power pack can be operated from an AC power source of either 105-125VAC or 210-240VAC 50/60 Hz. The appropriate AC power range is selected by jumper wires on the AC input terminal block mounted next to the power transformer inside the power pack. Figure 3.1 illustrates the connection of these jumper wires. (Note that the power pack has been tagged to indicate the range for which it was set up before shipment.)

WARNING

Disconnect AC power before removing the power pack cover or changing the AC power range or fuses. Replacement fuses should be of the specified value and type to insure continued fire hazard protection.

The main power fuse (F6) must be changed whenever the AC power range is changed. F6 is mounted inside the power pack next to the AC input terminal block (see figure 3.1 for fuse location and type).

3.6 Connecting to the AC Source

Before the power pack is connected to any AC power source, verify that it has been set for the appropriate AC input power range.

The AC power source must have its neutral side at or near earth ground, and be provided with a separate safety-earth conductor. In applications using the S205 power pack, the AC source must also be switchable since this supply is not provided with an AC line switch.

The AC appliance cord set supplied with the S159 power pack can be connected directly to a suitable 115VAC source having a three prong receptacle. It can be connected to a 230VAC source by using a plug cap with NEMA 6-15P specifications or equivalent.

The S205 power pack is provided with a 12" long AC input cable for connecting the power pack to an AC power barrier strip. The cable is terminated with slotted spade lugs which are .296" wide and will accomodate #6 screws. The color coding for the cable wires is as follows:

Black	Line (HI)
White	Neutral (LO)
Green (or green/yellow)	Safety-Earth (ground)

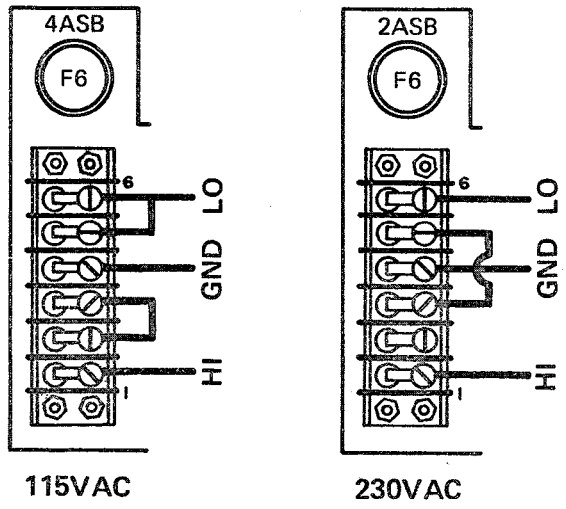


Figure 3.1 - AC Input Terminal Block
(115-230 VAC Input Selection)

4.0 FUSE REPLACEMENT AND VOLTAGE ADJUSTMENT

4.1 Fuse Replacement

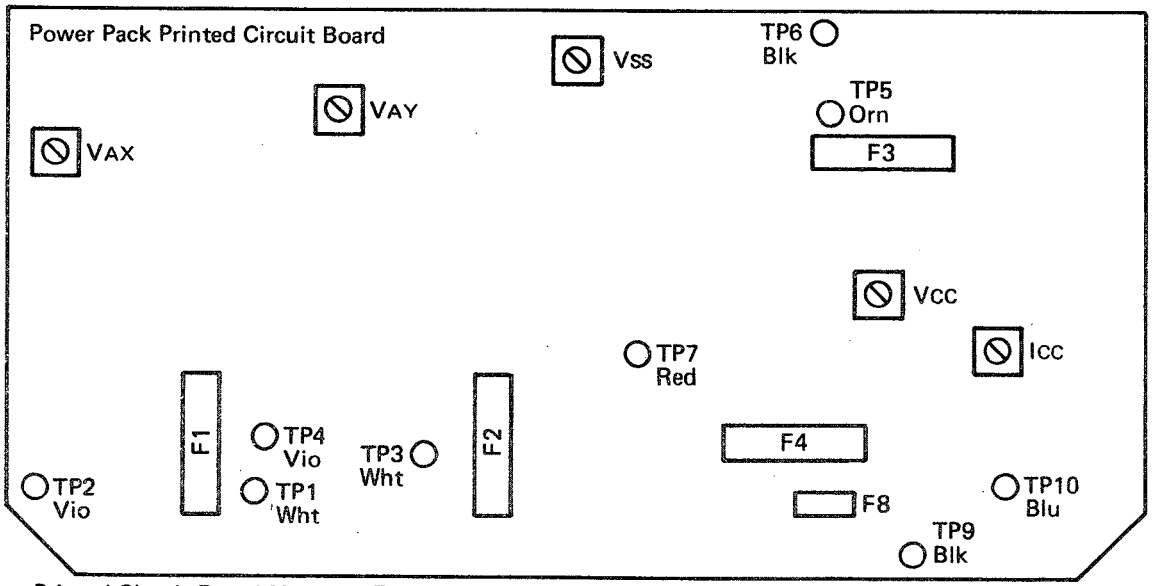
All fuses are mounted inside the power pack. See figure 4.1 for fuse locations and types.

CAUTION

Hazardous voltages exist inside the power pack. Disconnect AC power before removing cover or replacing fuses.

WARNING

When changing fuses, use only the value and type specified to insure continued fire protection.



Printed Circuit Board Mounted Fuses:

F1	VAX	.250 Ampere Normal Blow
F2	VAY	.250 Ampere Normal Blow
F3	VSB*	.600 Ampere Normal Blow
F4	VSS	.600 Ampere Normal Blow
F8	VSB	.375 Ampere Normal Blow

*Boost circuit

Chassis Mounted Fuses:

F5	VCC	5 Ampere Normal Blow
F6	115VAC	4 Ampere Slo-Blo
	230VAC	2 Ampere Slo-Blo
F7	VSC	3 Ampere Normal Blow

Voltage Test Points:

VAX	+TP2	-TP1
VAY	+TP4	-TP3
VSB	+TP5	-TP7
VSS	+TP7	-TP6
VCC	+TP10	-TP9

Figure 4.1 - Fuse, Test Point, and Adjustment Potentiometer locations

4.2 Voltage Adjustment

Generally, voltages may require readjustment when the power pack is used with an unpaired display, or after the display system has been in use for an extended period of time. The actual need for voltage readjustment is usually indicated when the display only partially writes or erases information. (The complete failure of the display to write or erase is generally caused by an interface or other circuit problem and does not necessarily mean the voltages require adjustment.)

Only V_{SS}, V_{AY} and V_{AX} should be readjusted; all other voltages are preset and should not be changed.

To adjust V_{SS}, V_{AY} and V_{AX}:

1) Disconnect AC power and remove the power pack cover (if so equipped)

CAUTION

Hazardous voltages exist inside the power pack. Disconnect AC power before removing the cover. Use caution when operating the power pack without its cover.

2) Connect a DC voltmeter to the appropriate test points, and using the appropriate potentiometers (see figure 4.1 for test point and potentiometer locations), adjust V_{SS}, V_{AY}, and V_{AX} to the levels specified on the blue system information card supplied with the display.

3) With the system set up for operation, reapply AC power and operate the display. Check for proper writing and erasing.

If the above procedure does not result in proper display operation:

It will be necessary to scan a pattern on the display so that approximately 25% of the light points are written. The pattern can be one generated specifically for voltage adjustments, or it can be a page of text or any other available material which approximates the 25% requirement.

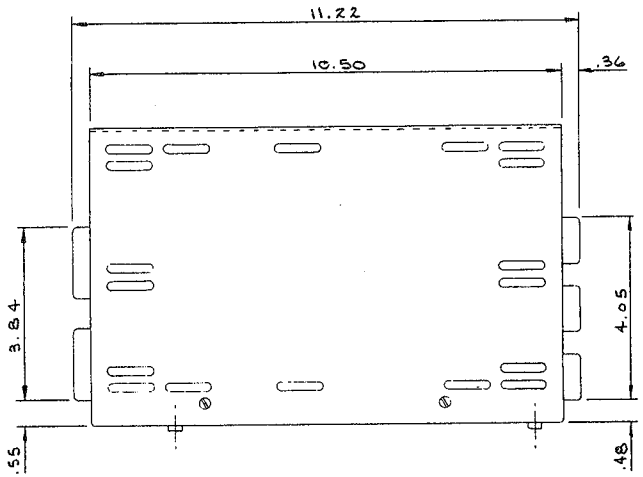
1) Remove AC power from the power pack and attach a DC voltmeter to the V_{SS} test points.

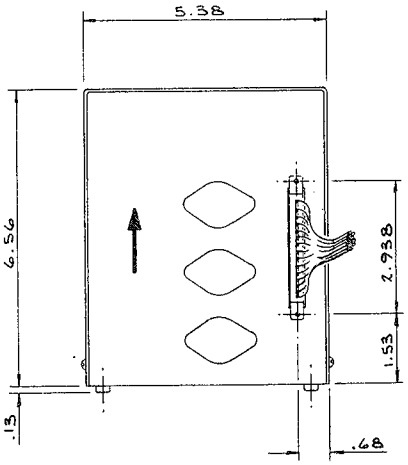
2) Reapply AC power and scan the display with the test pattern. Check for proper operation. If possible, selectively erase the test pattern and check for its complete erasure.

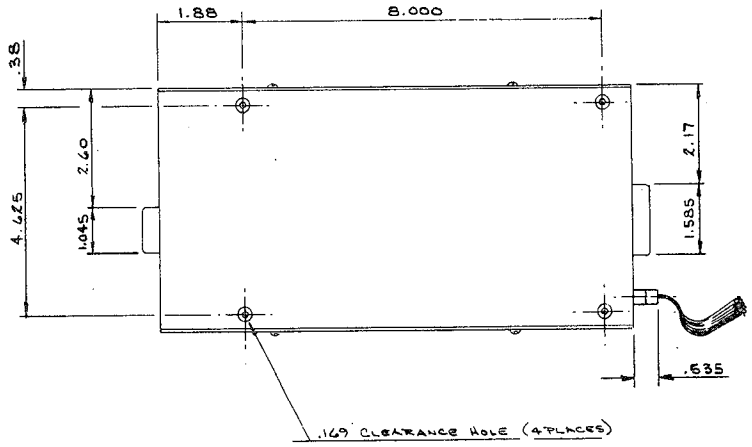
3) If some points fail to write when the pattern is scanned onto the display, V_{SS} is probably low. Slowly increase V_{SS} while repeatedly writing and erasing the test pattern (selective erase is preferable, but bulk erase may be used if necessary). Increase V_{SS} until the display operates properly then increase it one additional volt and record its final setting for reference (Adjustment complete)

4) If some points are being written that are not addressed, V_{SS} is probably too high. Decrease V_{SS} to approximately 85V, then slowly increase it using the procedure in step 3, above.

If there is any difficulty in adjusting voltages, contact our field service department at (419) 242-6543, ext. 66-217.







NOTE 2

COVER THICKNESS = .062

ARROW INDICATES MOUNTING POSITION, ARROW MUST POINT "UP"

.XX ±.02

.XXX ±.005

REF	ASSEMBLY		
E			
D			
C			
B			
A			
NO	REVISIONS	DATE	BY

TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL

DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS 5/16/74

TITLE MDXXXM / MID-V P. SUPPLY PHYSICAL CHARACTERISTICS

DRAWN	CHECKED	APPROVED	DATE
M.R.G.	FP	[illegible]	5-16-74

SCALE 1:2 DRAWING NO CP840M1200

MM61C

DIGIVUE®
MAINTENANCE MANUAL 512-60

POWER PACK
☐ S159
☐ S205

MM61C

DIGIVUE®
MAINTENANCE MANUAL 512-60

POWER PACK
☐ S159
☐ S205

Owens-Illinois Inc
Electro Optical Display Business Operations
Post Office Box 1035
Toledo, Ohio 43666
(419) 242-6543

Owens-Illinois, International S.A.
50, route des Acacias
1227 Carouge-Geneva, Switzerland
(022) 43 62 00

OWENS-ILLINOIS

$5.00

F

DIGIVUE® display/memory units are designed and produced for OEM (Original Equipment Manufacturer) applications, and as such are intended to be mounted in the purchaser's equipment or product. It is the responsibility of the purchaser to insure, as necessary, that the display unit and power pack are installed and used in accordance with Underwriter's Laboratories, government, or other applicable rules and regulations governing their end use (such as UL 114, NFPA pamphlet 75). Certain items which may be supplied with the display unit or power pack (e.g., cover, power switch, AC cord, etc.) are for the convenience of the purchaser only and are not intended to suggest possible uses for the display unit or power pack. Nor do they indicate that the display unit or power pack may be used as an end product as received by the purchaser without being incorporated into his equipment or in some way modified to meet the appropriate rules and regulations governing the end use of the display system.

Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document.

CONTENTS

ILLUSTRATIONS

1.0 INTRODUCTION

This manual is to be used in conjunction with the DIGIVUE® User Manual 512-60 Power Pack, UM609. Together these manuals provide detailed information relating to the operating principles, installation, and maintenance of the model 512-60 DIGIVUE® display/memory unit power pack, S159 and S205.

The emphasis in this manual is upon detailed descriptions of each voltage supply circuit used in the power pack, along with information useful in the troubleshooting and repair of these circuits.

2.0 POWER PACK ELECTRICAL CHARACTERISTICS

2.1 AC Input

102-127 VAC 50/60 Hz single phase 2.5 amperes
204-254 VAC 50/60 Hz single phase 1.25 amperes

2.2 DC Output Voltages

V_{CC}	4.8-5.25 VDC 3.75 amperes (with remote sensing)
V_{SC}	9 ±1 VDC 2 amperes
V_{AX}, V_{AY}	65-85 VDC 175 milliamperes
V_{SS}	85-105 VDC 500 milliamperes (maximum continuous) (700 milliamperes for intermittent periods)
V_{SB}	+38 ±2 VDC 50 milliamperes (for approximately 20 seconds after AC power is first applied, V_{SB} boosts to a level of approximately +120 ±10 VDC)

2.3 Line Regulation

V_{CC}	Less than 0.25% for a 102-127 VAC line change at rated load current
V_{AX}, V_{AY}, V_{SS}	Less than 0.1% for a 102-127 VAC line change at rated load current
V_{SC}, V_{SB}(boost)	Less than 20% for a 102-127 VAC line change at rated load current
V_{SB}(normal)	Less than 5% for a 102-127 VAC line change at rated load current

2.4 Load Regulation

V_{AX}, V_{AY}, V_{SS}	Less than 0.1% for a load current change equal to the current rating of the individual supply
V_{CC}	Less than 0.25% for a load current change equal to the current rating of the supply

2.4 Load Regulation - Continued

V_{SB}(normal)	Less than 5% for a load current change equal to the current rating of the supply
V_{SC}, V_{SB}(boost)	Less than 10% for a load current change equal to the current rating of the individual supply

2.5 Ripple and Noise

V_{CC}	Less than 50 millivolts peak to peak
V_{SC}	Less than 2 volts peak to peak
V_{AX}, V_{AY}, V_{SS}	Less than 100 millivolts peak to peak
V_{SB}	Less than 200 millivolts peak to peak

2.6 Over Current Protection

Line voltage	4 ampere/slow blow fuse - 115VAC (F6) 2 ampere/slow blow fuse - 230VAC (F6)
V_{CC}	Foldback current limiting and 5 ampere normal blow fuse (F5)
V_{SC}	3 ampere normal blow fuse (F7)
V_{AX}	Foldback current limiting and .25 ampere normal blow fuse (F1)
V_{AY}	Foldback current limiting and .25 ampere normal blow fuse (F2)
V_{SS}	Foldback current limiting and .6 ampere normal blow fuse (F4)
V_{SB}	.375 ampere normal blow fuse (F8) [.6 ampere normal blow fuse (F3) in boost circuit]

2.7 Adjustments

V_{CC}, V_{AX}, V_{AY}, V_{SS}, I_{CC}	Screwdriver voltage adjustment, printed circuit board mounted potentiometer
V_{SC}, V_{SB}	No adjustment (preset)

3.0 OPERATIONAL DESCRIPTION

(The following description should be accompanied by drawing DP340E0150.)

3.1 Input Circuitry

AC power is connected to the power pack through a terminal block which is mounted near the power transformer. The position of jumper wires on the terminal block determine the AC voltage range in which the power pack will operate. (See section 3.5 DIGIVUE® User Manual 512-60, UM609, for instructions regarding the selection of the AC input range.)

The power pack is protected against excessive input current by line fuse F6 (the rating for F6 varies with the AC input range selected). Thermal damage is prevented by a thermal switch mounted inside the power transformer. The thermal switch opens should the temperature of the transformer core exceed 120°C $\pm$ 5°C. (The thermal switch resets automatically.)

Voltage transients are suppressed by an LC filter composed of capacitors C33 and C34, and the inductance of the power transformer. Varistors RV1 and RV2 are also provided across the primary windings of the power transformer.

3.2 Control Voltage (V_{CC})

The control voltage source (V_{CC}) supplies 5 VDC to the control interface logic, address, and sustainer circuitry in the display.

The AC line voltage is stepped down to 16 VAC by the power transformer. This voltage is rectified by a full-wave bridge rectifier, CR54, and filtered by capacitor C25. The resulting 16 VDC is used to power the regulator integrated circuit, U4.

The voltage from the center tap of the power transformer's control voltage secondary winding is filtered by C32 and then connected to the series pass (Darlington) transistor Q7. The series pass transistor is controlled by the regulator, U4, which consists of an error amplifier and a reference source (see diagram of U4 on the schematic).

Resistors R53, R54, and R55 form a voltage divider which provides a 4.75-5.3 VDC reference voltage to the non-inverting input of the U4 error amplifier (the error amplifier is connected as a

voltage follower.) Capacitor C22 is used to reduce noise and ripple at the non-inverting input of the operational amplifier section of U4. Roll off and frequency compensation for the error amplifier are provided by capacitor C24.

The control voltage supply uses external sensing to compensate for lead length and voltage drops in the various conductors between the power supply and the load (display unit). The inverting input of the error amplifier is connected to the V_{CC} positive sensing terminal which in turn is connected(by way of the display power interconnect cable) to the output of the control voltage power supply. This voltage is compared, in the error amplifier, to the voltage supplied by the reference source. If there exists a difference in potential between these two voltages, the regulator will change the drive current to the series pass transistor, thereby holding the output of the control voltage supply constant. (The supply is designed to operate with a maximum lead length of 5 feet.) To avoid damage to the load, diodes CR51 and CR52 are provided to simulate sensor conductors should one of the sensor lines not be connected to the supply output.

The control voltage supply and its load are protected against external overloads through current foldback. The current foldback circuit consists of resistors R52, R56, R57, and R58; diode CR49; and a sense transistor located in U4. For normal operating conditions resistor R57 is adjusted to make the base-emitter junction of the sense transistor slightly positive. When the supply load current exceeds 4 amperes the voltage drop across the voltage divider (consisting of resistors R56, R57, and R58) increases, making the base of the sense transistor more positive; turning it on. This reduces the current to the series pass transistor Q7, which in turn reduces the output voltage and current. (When the output of the supply is short-circuited, the output current is reduced to approximately 300 milliamperes.) Removing the cause of the over current condition restores the supply to normal operation.

3.3 Addressing Voltages (V_{AX} and V_{AY})

The V_{AX} and V_{AY} supplies, providing voltages to the display address circuitry in the X and Y axes respectively, are electrically the same. Therefore, the following description of the section producing V_{AX} will apply to both supplies.

The positive address voltage supply (V_{AX}) circuit consists of a pre-regulator and a series regulator. The pre-regulator contains a main rectifier, a zener reference, and a filter capacitor. The main rectifier (full-wave bridge), which is composed of two silicon controlled rectifiers (CR4 and CR8) and two diodes (CR11 and CR13), rectifies the 80 VAC from the secondary of the power transformer. The resulting DC voltage, which can vary from 88-105 VDC depending upon line and load conditions, is filtered by capacitor C2 and applied to the collector of the series pass transistor Q3.

The pre-regulator minimizes the power losses in Q3 by maintaining a fixed voltage across its collector-emitter. The voltage $V_{AX} + V_Z$ (see figure 3.1) is used as a reference by the pre-regulator. When the voltage at the collector of Q3, with respect to V_{AX} common, is less than $V_{AX}+V_Z-V_{SCR}-V_D$, the silicon control rectifier with the positive potential at its anode will turn on and stay on until the potential is negative. This continues until the voltage at the collector of Q3 is greater than $V_{AX}+V_Z-V_{SCR}-V_D$.

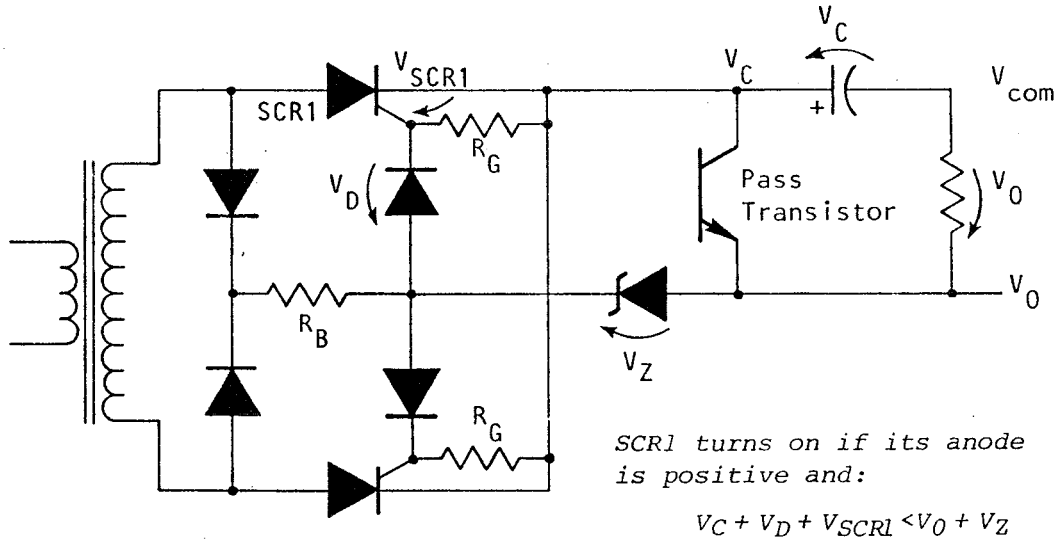


Figure 3.1 - Pre-Regulator Circuit

The linear series regulator uses an integrated circuit voltage regulator (U1) which contains a reference source, error amplifier, and a Darlington amplifier. Since V_{REF} (pin 6 of U1) equals 7 VDC, the divider network composed of R4 and R5 provides 3.5 volts, with respect to V_{AX}, to the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to a voltage divider network consisting of resistors R2, R3, and R7. Whenever there is a voltage change in the divider due to a change in the setting of the adjustment potentiometer R3, or a fluctuation in V_{AX} as a result of changing load conditions; the non-inverting input of the error amplifier is changed. This causes the output voltage (V_{AX}) to vary, which in turn causes the divider voltage drop to change until the difference in voltage between the inverting and non-inverting inputs of the error amplifier is zero.

Diodes CR1 and CR2 are used to clamp the inputs of the error amplifier at 0.6 volts or less. Diode CR3 prevents the error amplifier from latching due to parasitic capacitance in the circuit wiring. Capacitor C3 is used to insure correct biasing throughout the regulator circuit when the supply is turned on. Noise at the output of the regulator is prevented by filter capacitor C35.

The output of the regulator passes through an internal zener diode which shifts the output voltage of U1 to 6.2 volts in order to provide sufficient operating voltage to transistor Q3.

The supply output is protected against over current conditions by foldback current limiting. The foldback current limiting circuit consists of resistors R6, R8, and R14; output transistor Q3; and a sensing transistor located inside U1.

The input voltage to the base of the sense transistor is provided by a voltage divider connected between the V_{AX} output and common. During normal operation this voltage is less than 0.6 volts ($V_{R14} + V_{BE \text{ of } Q3} - V_{R8}$) and the sense transistor is off. When abnormal load conditions exist, this voltage exceeds 0.6 volts. This turns on the sense transistor, shunting some of the current from the base of the output transistor Q3, and causes the output voltage and current to fold back. Removing the cause of the current overload restores the supply to normal operation.

3.4 Sustainer Voltage (V_{SS})

The sustainer voltage (V_{SS}) is used to power the display matrix sustainer circuits; serves as a reference level for V_{SB} to power the border sustainer circuits; and provides the voltage from which the X and Y axis medium voltages (V_{MX} and V_{MY}) are derived. The sustainer voltage supply circuitry consists of a pre-regulator and a series regulator.

The pre-regulator consists of a main rectifier, a zener reference, a filter capacitor and an optical isolator. The main rectifier (full-wave bridge) is composed of two silicon control rectifiers (CR32 and CR44) and two diodes (CR36 and CR38). When the supply is first energized, the reference source is disconnected from the silicon control rectifiers by the optical isolator IS1; preventing the rectifiers from conducting until the V_{CC} supply voltage has climbed to 4.3 volts (see section 3.6, Level Detector). When this occurs, the level detector activates IS1 which in turn connects the zener reference source to the gates of the silicon control rectifiers. (Up to this time V_{SS} is zero.)

The main rectifier recrifies the 110 VAC from the secondary winding of the power transformer. The resulting DC voltage, which can vary from 99V to 136V depending upon line and load conditions, is filtered by capacitor C30 and applied to the collector of the series pass transistor Q6.

The pre-regulator minimizes the power losses in Q1 and Q6 by maintaining a fixed voltage across their collector and emitter. The reference voltage for the pre-regulator is equal to $V_{SS} + V_Z$ (see figure 3.1). When the voltage at the collector of Q6, with respect to V_{SS} common, is less than $V_{SS}+V_Z-V_{SCR}-V_D$, the silicon control rectifier that has a positive potential at its anode will turn on and stay on until the potential is negative. This continues until the voltage of the collector of Q6 is greater than $V_{SS}+V_Z-V_{SCR}-V_D$.

The series regulator uses an integrated circuit voltage regulator U3, which contains a reference source, error amplifier, and a Darlington amplifier. Since V_{REF} (pin 6 of U3) is equal to 7 VDC, the divider network composed of resistors R32 and R33 provides 3.5 VDC,with respect to V_{SS}, to the inverting input of the error amplifier. The non-inverting input of the error amplifier is connected to a voltage divider network consisting of resistors R29, R30, and $31. Changes in the setting of

the V_{SS} adjustment potentiometer, R29, or fluctuations in the V_{SS} level cause variations to occur in the reference voltage at the non-inverting input to the error amplifier. The supply automatically varies the level of V_{SS} until the inverting and non-inverting inputs to the error amplifier are once again balanced.

Diodes CR29 and CR30 are used to clamp the inputs of the error amplifier at 0.6 volts or less. Diode CR31 prevents the error amplifier from latching due to parasitic capacitance in the circuit wiring. Capacitor C15 is used to insure correct biasing throughout the regulator circuit when the supply is turned on. Noise at the output of the regulator is prevented by filter capacitor C37.

The output of the regulator passes through an internal zener diode which shifts the output voltage of U3 to 6.2 volts in order to provide sufficient operating voltage to transistors Q1 and Q6.

The supply output is protected against over current conditions by foldback current limiting. The foldback current limiting circuit consists of resistors R34, R36, R42, and R43; output transistor Q6; and a sensing transistor located inside U3. Positive feedback is introduced by an increase in current flow through resistors R13, R14, and R15 such as would result should a short circuit exist across the V_{SS} outputs. This causes the base-emitter junction of the sensing transistor inside U1 to be forward biased; removing the drive current to the internal Darlington amplifier. The actual amount of positive feedback provided depends upon the relationship between the current from the voltage drops across R4, R5, R13, and R15; and the base current of the sensing transistor. When the short circuit is removed, the full output voltage is restored.

The input voltage to the base of the sense transistor is provided by a voltage divider connected between the V_{SS} output and common. During normal operation, this voltage is less than 0.6 volts (V_{R42} + V_{BE} of Q6 - V_{R36}) and the sense transistor is off. When abnormal load conditions exist, this voltage exceeds 0.6 volts. This turns on the sense transistor, shunting some of the current from the base of the output transistor Q6, and causes the output voltage and current to fold back. Removing the cause of the current overload restores the supply to normal operation.

3.5 Border Supply (V_{SB})

The border supply provides the DC voltage to the border sustainer circuits. Since the border supply is referenced to the sustainer supply (V_{SS}), the actual voltage supplied to the border sustainer circuitry is equal to $V_{SS} + V_{SB}$.

When AC power is initially applied, isolator IS2 is energized (see section 3.7, Border Sequencer); providing a gate signal to the border boost rectifier, CR45. CR45, a half-wave rectifier, provides approximately 115 VDC which is filtered by capacitor C21. Since the boost voltage is greater than the voltage supplied by the border regulator, CR48 is back-biased and the boost voltage appears at the output of the supply. After approximately 15 seconds isolator IS2 is de-energized, and the voltage at the output of the supply drops until CR48 is no longer back-biased. Current is then supplied to the border sustainer circuits by the border regulator and the sustainer voltage supply ($V_{SS} + V_{SB}$).

The border regulator is a series regulator. the output of which is determined by the reference diode CR41, the base-emitter drop of Q5, and the forward drop of CR48. This output voltage is fixed at approximately 40 VDC.

The border supply is protected from overcurrent conditions by two fuses: F3 and F8. Fuse F3 protects the supply while it is in the boost state. Once the boost condition has passed, F8 takes over the protection of the regulator circuit.

Diode CR47 is used to protect the border and sustainer supplies should the border supply output be shorted to V_{SS} common. If this occurs, CR47 will be forward biased across the V_{SS} supply outputs. The V_{SS} supply will be forced to fold back, and fuse F8 in the border supply will open. (It is also possible that fuse F3 will open, particularly if the short occurs while the border supply is in the boost state.)

3.6 Level Detector

A level detector is used to sense the level of the control voltage (V_{CC}) to insure that it is at approximately 4.3 VDC before V_{SS} is applied to the sustainer circuits. (This circuit is part of the V_{CC} supply.)

When AC power is first applied and the control voltage (V_{CC}) output level is low, the voltage drop across resistor R61 is not sufficient to cause the zener diode

CR59 to conduct, and transistor Q2 is not turned on. (The lamp in isolator IS1 remains off.) When V_{CC} reaches approximately 4.3 VDC, the zener diode CR59 conducts;

turning on Q2 which in turn turns on the lamp in IS1. The change in resistance in IS1 as a result of the glowing lamp, activates the gate circuit for CR32 and CR41, energizing the sustainer voltage supply. Capacitor C28 delays the turn on of the V_{SS} supply for approximately 30 milliseconds, which gives the V_{CC} supply time to stabilize.

3.7 Border Sequencer

The border sequencer circuit automatically increases the voltage to the border sustainer circuits ($V_{SS}+V_{SB}$) to approximately 200 VDC for approximately 20 seconds after AC power is first applied. (This circuit is part of the V_{CC} supply.)

The time period during which the voltage to the border sustainers is boosted is controlled by U5 (NE555) (see figure 3.2). Initially, C27 is prevented from charging

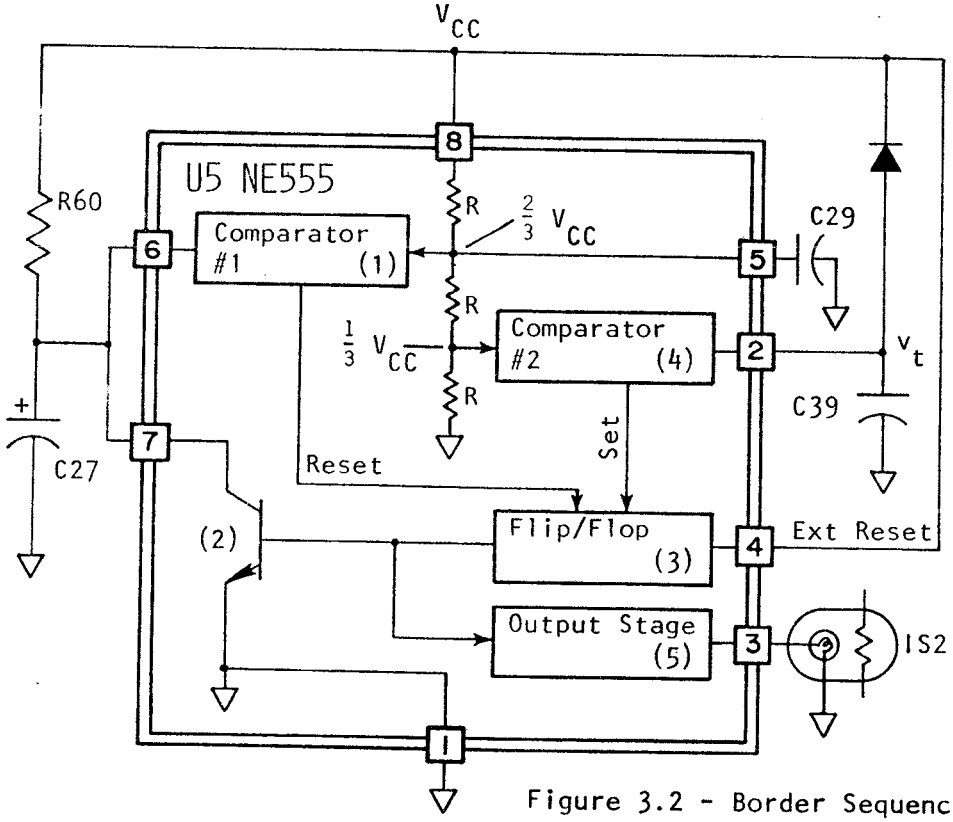


Figure 3.2 - Border Sequencer

by transistor (2) which is turned on. When the control voltage supply is first energized, pin 2 of U5 is momentarily pulled to V_{CC} common by the current flowing into capacitor C39. This LO going pulse sets the flip-flop (3); turning off transistor (2) and causing the output stage (5) to go HI. The output stage (5) turns on the lamp in isolator IS2, which causes an increase in the output voltage produced by the border voltage supply (as described in section 3.5). Capacitor C27 is allowed to charge. When the voltage across C27 is equal to approximately 2/3 of V_{CC}, the comparitor (1) resets the flip-flop (3); turning on transistor (2) once more. This causes C27 to discharge and also turns off the output stage (5) and, in turn, the lamp in isolator IS2. $V_{SS}+V_{SB}$ returns to its normal operating level. (Diode CR53 is used to discharge C39 to reduce recycling time.)

4.0 MAINTENANCE

4.1 Voltage Monitoring

Test points have been provided in the power pack for monitoring voltage levels. These test points are located on the main printed circuit board and are accessible by removing the power pack cover. Figure 4.1 illustrates the locations of the test points, their color codes, and the voltage associated with each. Test points are not provided for V_{SC}. This voltage can be measured across C32 (see drawing DP340M1300 for location).

WARNING

Hazardous voltages exist inside the power pack. Disconnect AC power before removing the cover.

CAUTION

AC power may be applied to the power pack while it is disconnected from the display module. However, do not attempt to reconnect the power pack to the display module without first removing AC power and allowing 10 seconds for the output voltage levels to return to zero.

To monitor voltages with the power pack disconnected from its load, short out diodes CR51 and CR52 on the power pack printed circuit board.

When making voltage measurements, it is recommended that a measuring device with a meter movement readout be used.

4.2 Voltage Adjustment

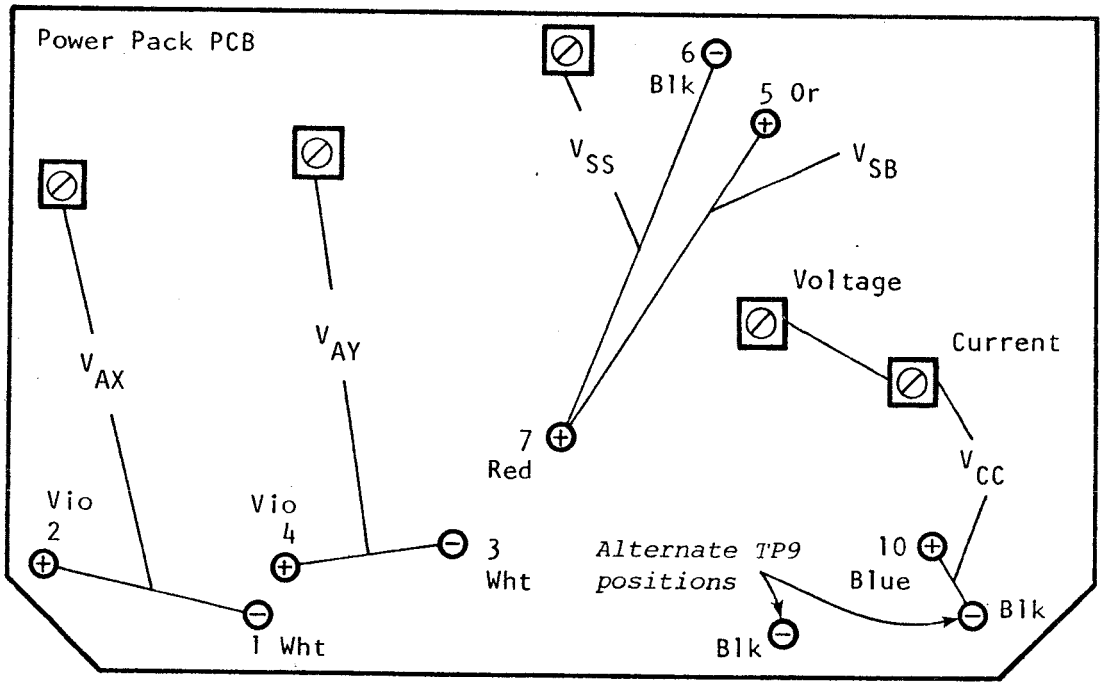
The procedure for adjusting V_{SS} is given in UM609. To adjust the remaining voltages that are adjustable (V_{CC}, V_{AX}, V_{AY}):

WARNING

Hazardous voltages are present inside the power pack. Disconnect the power pack from the AC power source before removing the cover. Use caution when operating the power pack with the cover removed.

1) Remove the cover from the power pack.

2) Attach a suitable DC voltmeter to the test points associated with the voltage to be adjusted (see figure 4.1 for test point locations).



* Measure V_{SC} across C32

Figure 4.1 - Adjustment Potentiometer and Test Point Locations

3) Attach the power pack output cable to the D141 display unit to provide proper loading. (Power pack voltages can be

adjusted without the display attached by shorting out diodes CR51 and CR52 on the power pack PCB. However, using this method, the voltages may change when a load is subsequently applied.)

4) Apply AC power.

5) Locate the appropriate adjustment potentiometer for the voltage being adjusted (see figure 4.1) and adjust the voltage to the level indicated:

V_{CC}	5 VDC (may be set one or two tenths of a volt higher if the maximum length power interconnect cable (5 feet) is being used).
V_{AX} & V_{AY}	80 VDC

6) Remove AC power and replace cover.

4.3 V_{CC} Current Limit Adjustment

The V_{CC} current limit has been pre-adjusted, and should not be readjusted unless necessary. To readjust the V_{CC} current limit, proceed as follows:

> WARNING
>
> Hazardous voltages are present inside the power pack. Disconnect the power pack from the AC power source before removing the cover. Use caution when operating the power pack with the cover removed.

1) Remove the cover from the power pack.

2) Attach an adjustable 2 or 3 ohm, 25 watt resistor to the output of the V_{CC} supply (be sure to connect the sense lines to the output also). Adjust the resistor for maximum resistance.

3) Attach a suitable DC voltmeter to measure V_{CC} at the load. (The use of a digital voltmeter is recommended for this adjustment.)

4) Attach a clamp-on DC ammeter to measure the load current.

5) Connect the power pack to an auto-transformer. Apply AC power and adjust the line voltage to 115 VAC.

6) Set the V_{CC} current limit adjustment potentiometer, R57, maximum clockwise (see figure 4.1 for potentiometer location).

7) Adjust the load resistor for a load current of 4 amperes.

8) Slowly turn the V_{CC} current limit adjustment potentiometer counterclockwise until the output voltage starts to decrease. The current limit is now set. Do not change the potentiometer setting.

9) Decrease the load resistance to zero; the maximum load current should be less than 300 milliamperes.

10) Remove AC power and replace the cover.

4.4 Fuse Replacement

See DIGIVUE® User Manual, 512-60 Power Pack S159, UM609; for fuse types, locations, and replacement procedures.

4.5 Troubleshooting Charts

Start on Next Page

Troubleshooting charts for each voltage section of the power pack are given on the following pages.

POWER PACK

- *No power to display unit*

NOTE: Disconnect power pack from display unit and short diodes CR51 and CR52 to close sense leads when troubleshooting supply.

Check AC line voltage

- *No AC line voltage*

Check external circuits

- *AC line voltage OK*

Check fuse F6

- *Fuse F6 open*

Check for shorted capacitors: C2, C7, C9, C14, C20, C21, C30, C32, C33, C34

Check for shorted varistors: RV1, RV2

Check for shorted diodes: CR9, CR11, CR12, CR13, CR24, CR25, CR26, CR27, CR35, CR36, CR37, CR38, CR47, CR54

Check for shorted SCR's: CR4, CR8, CR18, CR21, CR32, CR44

Check for shorted transformer windings (primary and/or secondary)

- *Fuse F6 OK*

Check transformer secondary voltages

- *No secondary voltages*

Check for defective thermal switch in transformer primary

Check for unusually high operating temperature

- *Secondary voltages OK*

Check individual regulator sections

V_{CC} REGULATOR SECTION

Measure DC voltage from TP10 to TP9

NOTE: Use a 1.34Ω, 25 watt resistor as load when troubleshooting this section.

- *Poor regulation*

  Check for defective regulator U4

  Check for shorted capacitors: C23, C24

  Check for shorted diode CR54

- *Voltage lower than 4.8 VDC*

  Check fuse F5

  - *Fuse F5 OK*

    Check resistor R53 adjmt

    Check for shorted capacitors: C22, C23, C24

    Check transistor Q7

    Check for defective regulator U4

    Check for open transformer secondary

  - *Fuse F5 open*

    Check transistor Q7

- *Voltage higher than 5.25 VDC*

  Check resistor R53 adjmt

  Check for defective regulator U4

  Check for open resistors: R53, R54, R55

  Check transistor Q7

- *Current foldback*

  Under sensitive

  Check resistor R57 adjmt

  Check for defective regulator U4

  Check for open resistor R56

  - *Over sensitive*

    Check resistor R57 adjmt

    Check for defective regulator U4

    Check for shorted diode CR49

    Check for open resistors: R52, R57, R58

V_{SC} REGULATOR SECTION

Measure DC voltage from pin 15 of J1 to TP9

NOTE: Use a 4Ω, 25 watt resistor as load when troubleshooting this section.

•*Voltage less than 8 VDC*

Check fuse F7

•*Fuse F7 OK*

Check for shorted capacitor C32

•*Fuse F7 open*

Check for trouble in display unit

V_{AX} REGULATOR SECTION

Measure DC voltage from TP2 to TP1

NOTE: Use a 500Ω, 25 watt resistor as load when troubleshooting this section.

- *Poor regulation*
  - Check for shorted diodes: CR1, CR2, CR3, CR14
  - Check for shorted SCR's: CR4, CR8
  - Check for defective regulator U1
  - Check for shorted capacitor C5
- *Voltage lower than 65 VDC*
  - Check fuse F1
    - *Fuse F1 OK*
      - Check resistor R3 adjmt
      - Check for defective regulator U1
      - Check for shorted capacitors: C1, C5, C6
      - Check for open resistors: R4, R5, R9, R12, R14
      - Check for shorted diode CR5
      - Check transistor Q3
      - Check for open transformer secondary
    - *Fuse F1 open*
      - Check transistor Q3
      - Check for shorted diode CR14
      - Check for shorted capacitor C1
- *Voltage higher than 85 VDC*
  - Check resistor R3 adjmt
  - Check for open resistors: R2, R3, R7
  - Check for defective regulator U1
  - Check for shorted diode CR14
  - Check transistor Q3
- *Current foldback*
  - *Under sensitive*
    - Check for defective regulator U1
    - Check for open resistors: R8, R9
    - Check for shorted capacitor C4
    - Check transistor Q3
  - *Over sensitive*
    - Check for open resistors: R6, R14
    - Check for open capacitor C4
    - Check for defective regulator U1

V_{AY} REGULATOR SECTION

Measure DC voltage from TP4 to TP3

NOTE: Use a 500Ω, 25 watt resistor as load when troubleshooting this section.

•Poor regulation

Check for shorted diodes: CR15, CR16, CR17, CR28

Check for shorted SCR's: CR18, CR21

Check for defective regulator U2

Check for shorted capacitor C12

•Voltage lower than 65 VDC

Check fuse F2

•Fuse F2 OK

Check resistor R17 adjmt

Check for defective regulator U2

Check for shorted capacitors: C8, C12, C13

Check for open resistors: R18, R19, R22, R26, R28

Check for shorted diode CR23

Check transistor Q4

Check for open transformer secondary

•Fuse F2 open

Check transistor Q4

Check for shorted diode CR28

Check for shorted capacitor C8

•Voltage higher than 85 VDC

Check resistor R17 adjmt

Check for open resistors: R16, R17, R21

Check for defective regulator U2

Check for shorted diode CR28

Check transistor Q4

•Current foldback

•Under sensitive

Check for defective regulator U2

Check for open resistors: R22, R23

Check for shorted capacitor C11

Check transistor Q4

•Over sensitive

Check for open resistors: R20, R28

Check for open capacitor C11

Check for defective regulator U2

V_{SS} REGULATOR SECTION

Measure DC voltage from TP7 to TP6

NOTE: Use 270Ω, 100 watt resistor as load when troubleshooting this section.

•Poor regulation

Check for shorted diodes: CR29, CR30, CR31

Check for defective regulator U3

Check for shorted capacitor C17

Check for shorted SCR's: CR32, CR44

•Voltage lower than 85 VDC

Check fuse F4

•Fuse F4 OK

Check for defective regulator U3

Check transistors: Q1, Q6

Check for shorted capacitors: C17, C18, C31

Check for open resistors: R32, R33, R37, R42, R43, R51, R61

Check optical isolator IS1

Check resistor R29 adjmt

Check for open transformer secondary

•Fuse F4 open

Check transistor Q6

Check for shorted capacitor C31

Check for shorted diode CR42

•Voltage higher than 105 VDC

Check for defective regulator U3

Check transistors: Q1, Q6

Check resistor R29 adjmt

Check for open resistors: R29, R30, R31

Check for shorted diode CR42

•Current foldback

•Under sensitive

Check for defective regulator U3

Check transistors Q1, Q6

Check for open resistors: R36, R37, R44

Check for shorted capacitor C16

•Over sensitive

Check for defective regulator U3

Check for open resistors: R34, R42, R43

Check for open capacitor C16

V_{SB} REGULATOR SECTION

Measure DC voltage from TP5 to TP7 as AC voltage is applied

NOTE: Use a 3600Ω, 12 watt resistor as load when troubleshooting this section.

- *No boost voltage*

  Check fuse F3

  - *Fuse F3 OK*

    Check for defective timer U5

    Check optical isolator IS2

    Check resistors: R48, R49

    Check SCR CR45

    Check for open transformer secondary

    Check for shorted capacitor C21

    Check for shorted diode CR47

  - *Fuse F3 open*

    Check for trouble in display unit

- *V_{SB} (Normal) > 42 VDC*

  Check for defective timer U5

  Check optical isolator IS2

  Check for shorted capacitor C27

  Check for open resistor R60

- *V_{SB} (Normal) < 39 VDC*

  Check for shorted capacitors C19, C21

  Check for shorted diodes: CR41, CR47

  Check for open picofuse F8

4.6 Troubleshooting the V_{AX}, V_{AY}, or V_{SS} Pre-regulator

If a defective pre-regulator circuit (associated with V_{AX}, V_{AY}, or V_{SS}) is indicated by the absence of voltage from the pre-regulator output, the circuit can be quickly checked by using the following procedure:

> WARNING
>
> Hazardous voltages are present inside the power pack. Disconnect the power pack from the AC power source before removing the cover. Use caution when operating the power pack with the cover removed.

1) Remove AC power from the power pack and disconnect the power pack from the display.

2) Remove the power pack cover.

3) Locate the zener reference diode associated with the suspected defective circuit (V_{AX} CR5, V_{AY} CR23, V_{SS} CR33). Disconnect one end of the diode from the circuit.

4) Reapply AC power and observe the waveform across the filter capacitor at the output of the circuit (V_{AX} C2, V_{AY} C9, V_{SS} C30):

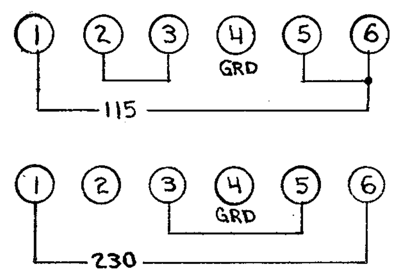
   a) If the waveform is filtered 120 Hz ripple, an indication that the circuit itself is okay, check for a shorted zener reference diode.

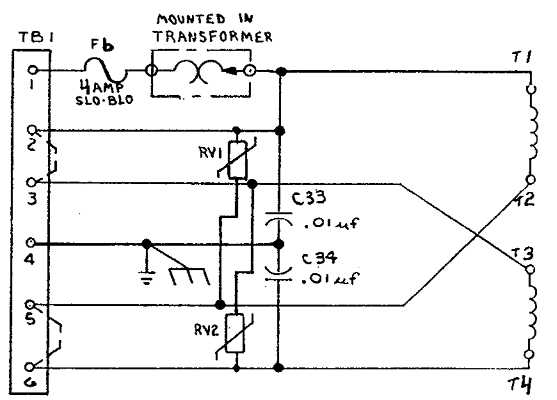
   b) If the waveform is filtered 60 Hz ripple, check for a defective SCR or other component in one leg of the circuit.

   c) If the waveform is 0 volts, check for both legs of the circuit being defective or a bad diode in the bridge circuit. (In V_{SS} circuit check for presence of V_{CC} and verify operation of IS1.)

4.7 Electronic and Mechanical Drawings (Parts Lists)

TERMINAL BLOCK CONNECTION (EXTERNAL)





1. AS SHOWN WIRED FOR 115VAC.
2. REMOVE JUMPERS 2 to 3 and 5 to 6 and ADD JUMPER 3 to 5 FOR 230VAC.
3. FUSE F6 TO BE 4A SLO-BLO FOR 115VAC OR 2A SLO-BLO FOR 230VAC.

NOTE:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE 1/4 W
   B. " " " ±10%
   C. " CAPACITORS ARE IN uf
   D. SECONDARY TRANSFORMER VOLTAGE ARE SHOWN WITH PRIMARY AT 100VAC.

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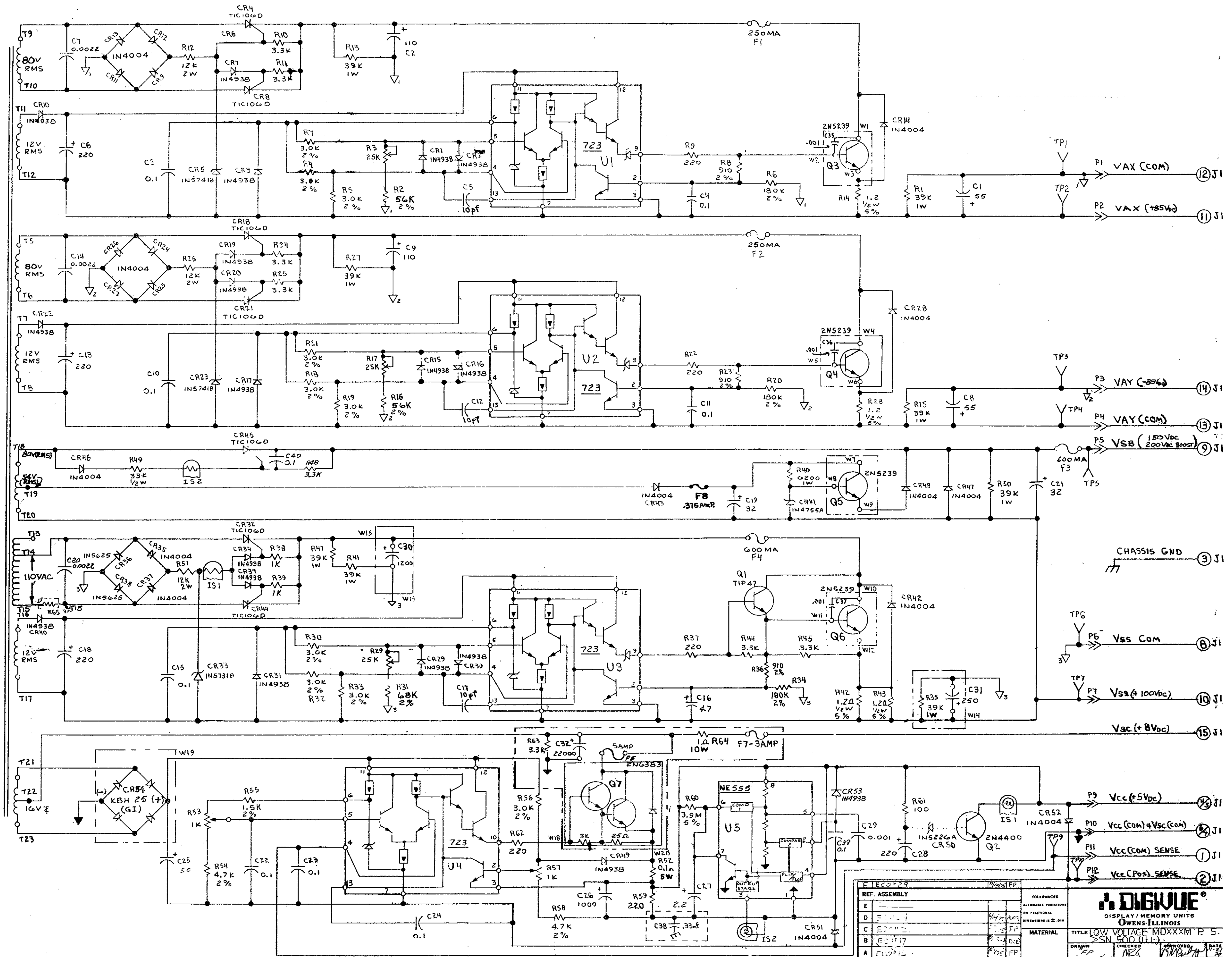


NO	REVISIONS	DATE	BY
G	ECO # 37		FP
F	ECO # 29		FP
E			
D			
C			
B			
A			

REF. ASSEMBLY

DIGIVUE DISPLAY/MEMORY UNITS Owens-Illinois

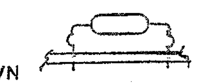
TITLE: LOW VOLTAGE MDXXXM P.S. SN 500 (U.L.)

DRAWN: FP — DRAWING NO. DP340E0150G

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
Q1	1	TRANSISTOR	T.I./G.E.	TIP47/D44R1
Q2	1	TRANSISTOR	MOT/FAIRCHILD	2N4400
U1,2,3,4	4	I.C. REGULATOR	FAIR/MOT/RAY/NAT/SIG	723PC
U5	1	I.C.	SIGNETICS	NE555V
F1,2	2	FUSE 250 M.A. N.B.	LITTLEFUSE	312.250
C4,11,24,39	4	.1MFD @50V +80% -20%	CENTRALAB	CY20C104P
F3,F4	2	" 600 " N.B.	"	312.600
R1,13,15,27,41,47,50	7	RESISTOR 1W 39K 10%	A.B.	RCR32
R40	1	" " 6.2K "	"	RCR32
R12,26,51	3	" 2W 12K "	"	RCR42
R31	1	" .25W, 68K, 2%	CORNING ELEC.	C4
R4,5,7,18,19,21,30,32	10	" " 3.0K "	" "	"
R33,56		" " " "	" "	"
R6,20,34	3	" " 180K "	" "	"
R8,23,36	3	" " 910Ω "	" "	"
R2,16	2	" " 56K "	" "	"
R10,11,24,25,44	8	" " 3.3K 10%	A.B.	RCR07
R45,48,63		" " " "	"	"
R59,R9,22,37,62	5	" " 220Ω "	"	"
C5,12,17	3	10PFD 1000WVDC ±20%	SPRAGUE	5GA-Q10
CR9,11-14,24-28,37,35	19	DIODE	GI/T.I./I.T.T.	1N4004
CR42,43,46-48,51,52		"	" " "	"
CR4,8,18,21,32,44,45	7	SCR	TI/RCA	TIC106D
CR36,38	2	DIODE	GI/GE	1N5625
R38,39	2	RESISTOR,.25W 1K 10%	A.B	RCR07
F8	1	PICOFUSE 3/8A, 125V	LITTLE FUSE	275.375
C16	1	4.7 MFD.@10V	KEMET	T362A475M010AS

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
R55	1	RESISTOR,.25W 1.5K 5%	CORNING ELEC.	C4
R54,58	2	" " 4.7K "	" "	C4
R61	1	" " 100Ω "	A.B	RCR20
R14,28,42,43	4	" .5W 1.2Ω 5%	A.B.	RCR20
R52	1	" 5W 0.1Ω 10%	CLAROSTAT	VC5E
R49	1	" .5W 33K "	A.B.	RCR20
R60	1	" .25W 3.9M 5%	"	RCR07
R3,17,29	3	POT. .5W 25K 10%	BECKMAN INSTR.	72P OR 72PM
R53,57	2	" " 1K "	" "	"
C1,8	2	CAP. 55µf @ 150V	SANGAMO	052FJ550W150B
C2,9	2	" 110µf @ 200V	"	057GP111T200B
C3,10,15,22,23,40	6	" .1µf @ 12V	CENTRALAB	XXUK-12-104
C29	1	" 0.001µf@1000V	SPRAGUE	C023B102E102P
C6,13,18,28	4	" 220µf @ 25V	MEPCO	ET221X025A00
C7,14,20	3	" .0022µf@1.4KV	CENTRALAB	C1-222
C19,21	2	" 32µf @ 250V	MEPCO	C436AR/M32
C25	1	" 50µf. @ 25V	SPRAGUE	TVA1206
C26	1	" 1000µf @ 10V	MEPCO	ET102X010A01
C27	1	" 2.2µf @ 40V	MEPCO	ET2P2X040A1
CR1-3,6,7,10,15-17,19,20	20	DIODE	TI/ITT	1N4938/ 2002
CR22,29,30,31,34,39		"		" "
CR40,49,53		"		" "
CR5,23	2	"	AMPEREX	1N5741B

KINK LEADS IN DIODES AS SHOWN



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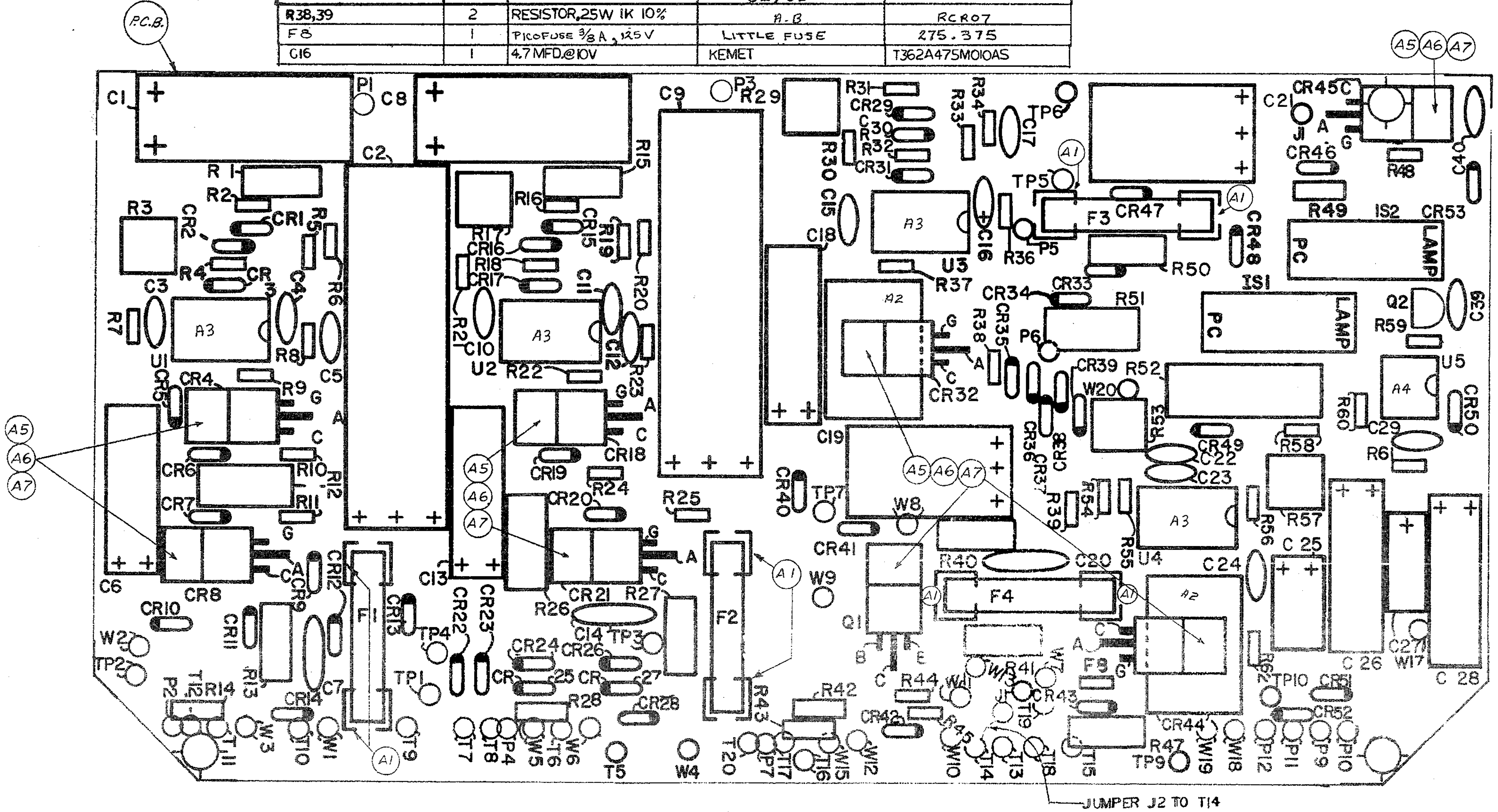
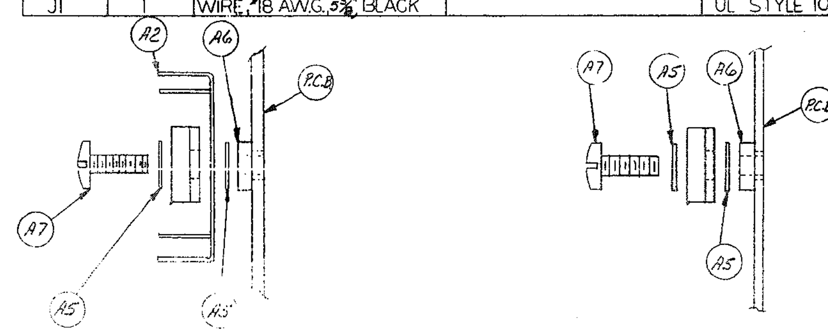
NOTES:
1. ZINC PLATE PER ZINC DICHROMATE SPEC 210MO200A TYPE II, CLASS 2
2. SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220MO300

SYM	QTY	DESCRIPTION	VENDOR	PART NO.
CR41	1	DIODE	MOTOROLA	1N4755A
CR33	1	"	AMPEREX	1N5731B
CR50	1	"	MOTOROLA	1N5226A
IS1,2	2	ISOLATOR, OPTO	SIGMA	301T1-6B1
TP2,4	2	TEST POINT VIOLET	E.F. JOHNSON	105-0862-001
TP7	1	" " RED	"	105-0852-001
TP5	1	" " ORANGE	"	105-0856-001
TP1,3	2	" " WHITE	"	105-0851-001
TP6,9	2	" " BLACK	"	105-0853-001
TP10	1	" " BLUE	"	105-0860-001
A1	8	FUSE HOLDER	LITTLE FUSE	102068
A2	2	HEAT SINK	IERC	PA1-1
A3	4	IC SOCKET 14PIN	AUGAT	314-AG5 D2R
A4	1	" " 8PIN	CAMBION	703-3772-01-04-16
A5	16	LOCKWASHER, INTERNAL TOOTH #4 - ZINC PLATE		
A6	8	THREADED BUSH. 4-40	USECO	9004B-NO PLATE
A7	8	SCREW, 4-40 X 1/4, PANHEAD - ZINC PLATE		
J2	1	WIRE, 18 A.W.G., 2" BLACK		UL STYLE 1007 PREFUSED
P.C.B.	1	P.C. BOARD		DP340D0100D
J1	1	WIRE, #18 A.W.G. 5⅝" BLACK		UL STYLE 1007





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D	ECO #24 & 26	6/2/75	MRG
C	ECO #18 + #20	2/14/75	FP

ASSEMBLY MDXXXD

TOLERANCES

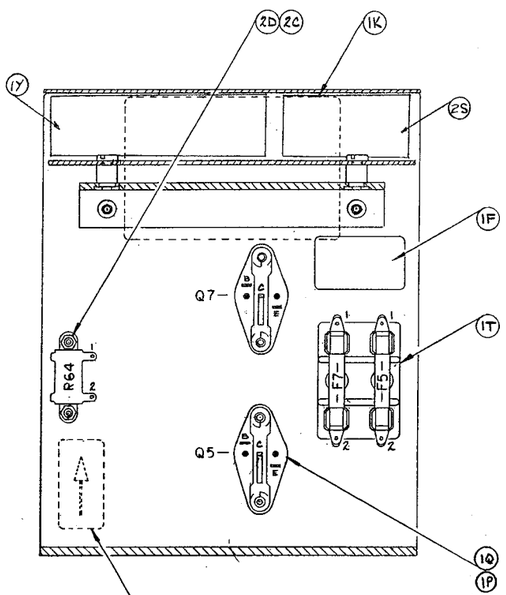
MATERIAL

DIGIVUE®
DISPLAY MEMORY UNITS
OWENS-ILLINOIS

TITLE LOW [illegible] (UL)

DRAWN | CHECKED MRG | APPROVED RCM | DATE

SCALE 2X | DRAWING NO. [illegible]



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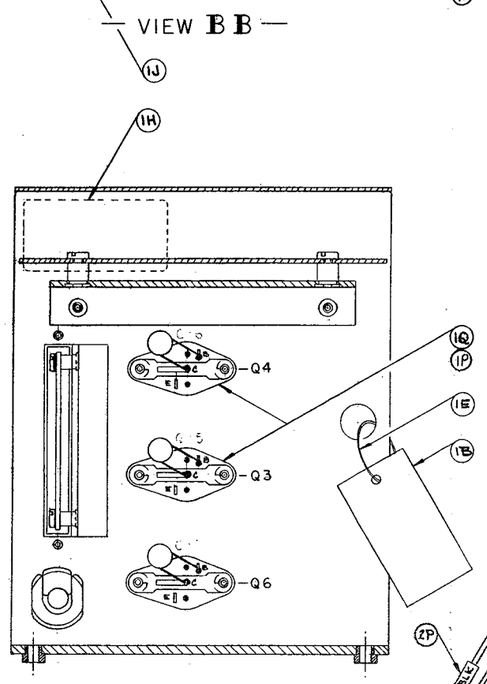

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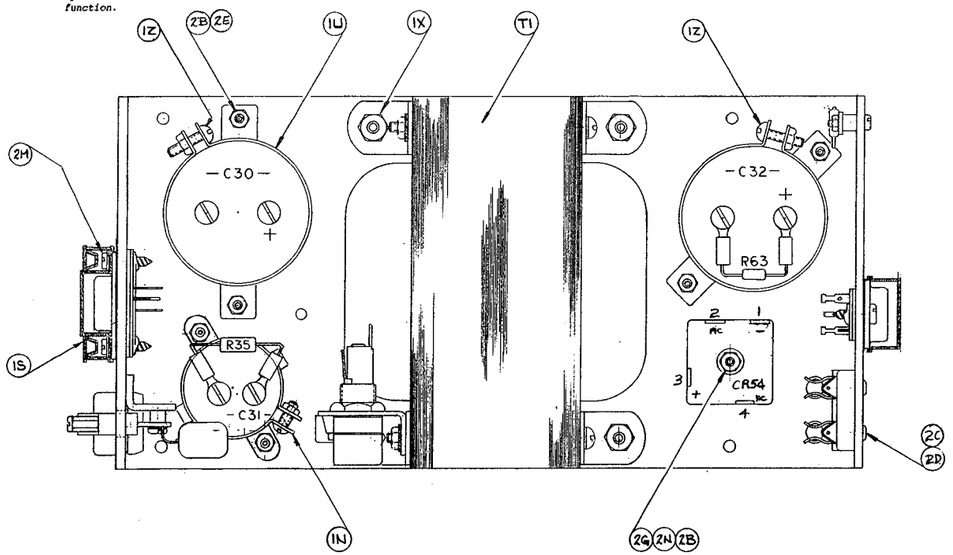
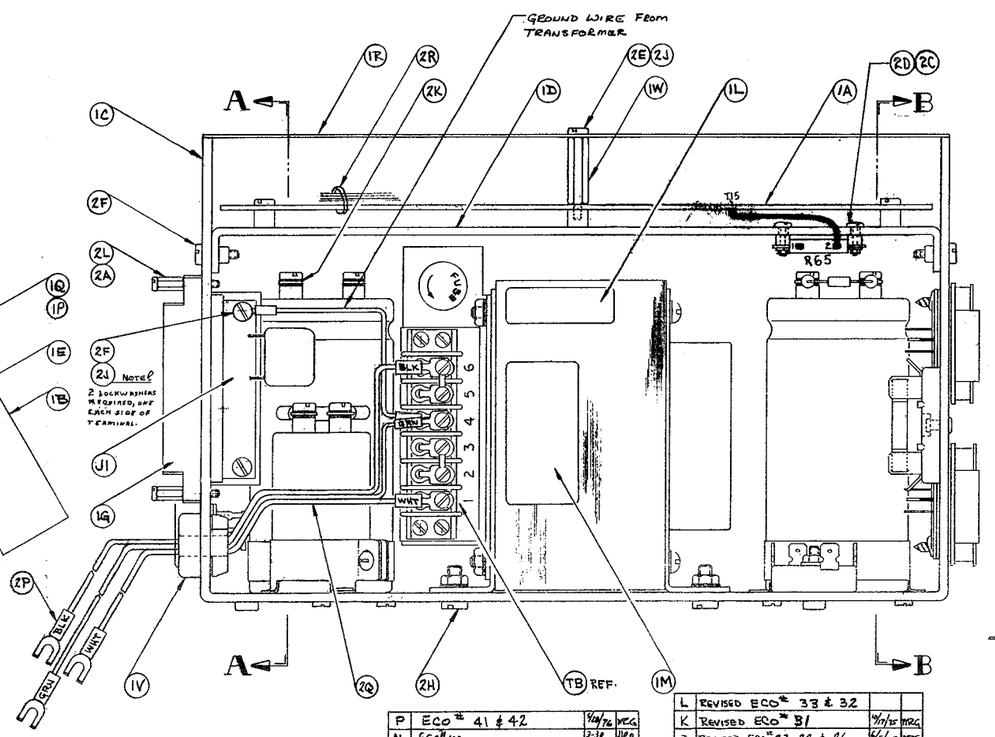
NOTE:
SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

NOTE:
ZINC PLATING PER ZINC DICHROMATE SPEC 210M0200A TYPE II CLASS 2.





P	ECO# 41 & 42	9/19/74	MEG.
N	ECO# 48	7-30-74	WB
M	ECO# 35	7/26/74	MEG.
NO.	REVISIONS CONT'D.	DATE	BY

L	REVISED ECO# 33 & 32		
K	REVISED ECO# 31	9/19/73	MEG.
J	REVISED ECO# 23, 24 & 26	6/6/73	MEG.
H	REVISED ECO# 15, 17	3/4/73	MEG.
NO.	REVISIONS CONT'D	DATE	BY

WIRING LIST

TERM. POINTS		AWG GAGE	AVG. LENGTH	REMARKS	WIRE COLOR
PCB-W1	Q3-C	18	7"		W/RED
PCB-W2	Q3-B	"	8"		W/GREEN
PCB-W3	Q5-E	"	7"		VIOLET
PCB-W4	Q4-C	"	8"		W/RED
PCB-W5	Q4-B	"	8"		ORANGE
PCB-W6	Q4-E	"	8"		BROWN
PCB-W7	Q5-C	"	10"		W/ORANGE
PCB-W8	Q5-B	"	12"		WHITE
PCB-W9	Q5-E	"	12"		ORANGE
PCB-W10	Q6-C	"	12"		W/ORANGE
PCB-W11	Q6-B	"	13"		W/GREEN
PCB-W12	Q4-E	"	12"		GRAY
PCB-W13	C30−	"	9"		W/YELLOW
PCB-W15	C30+	"	9"		W/RED
PCB-W17	C32−	"	9"		BROWN
PCB-W18	Q7-B	"	6"		GREEN
PCB-W19	CR54-3	"	9"		WHITE
PCB-W20	Q7-E	"	9"		BLUE
F5-1	Q7-C	"	4"		GRAY
F5-2	C32+	"	7"		RED
R64-1	C32+	"	3"		YELLOW
R64-2	F7-1	"	6"		GRAY
CR54-1	C32−	"	6"	(1) 31889 TERM. (1) 42599-2 TERM.	RED
F7-2	J1-15	18	19"		YELLOW
R35	C31−			(1) 31889 TERM.	
R35	C31+			" " "	
R63	C32−			" " "	
R63	C32+			" " "	
PCB-P1	J1-12	18	13"		VIOLET
PCB-P2	J1-11	"	6"		VIOLET
PCB-P3	J1-14	"	13½"		W/BROWN
PCB-P4	J1-13	"	8"		BROWN
PCB-P5	J1-9	"	11"		W/BLACK
PCB-P6	C31−	"	12"		W/YELLOW
PCB-P7	C31+	"	9"		RED
J1-8	C31−	"	3"		W/YELLOW
J1-10	C32+	"	3"		WHITE
PCB-P9	J1-4	"	13"		BLUE
PCB-P10	J1-6	"	13"		W/BROWN
PCB-P11	J1-1	"	13"		W/BLACK
PCB-P12	J1-2	18	13"		GREEN
TB-4	G1	18	3½"		GREEN
PCB-T15	R65-2	18	2"		RED

TRANSFORMER WIRING LIST

TERM. POINTS		GAGE	LENGTH	REMARKS	COLOR
T1-5	PCB-T5	22			BROWN
T1-6	PCB-T6	"			BROWN
T1-7	PCB-T7	"			WHITE
T1-8	PCB-T8	"			WHITE
T1-9	PCB-T9	"			VIOLET
T1-10	PCB-T10	"			VIOLET
T1-11	PCB-T11	"			WHITE
T1-12	PCB-T12	"			WHITE
T1-13	PCB-T13	"			RED
T1-14	PCB-T14	"			W/RED
T1-15	R65-1	"			RED
T1-16	PCB-T16	"			WHITE
T1-17	PCB-T17	"			WHITE
T1-18	PCB-T18	"			ORANGE
T1-19	PCB-T19	"			ORANGE
T1-20	PCB-T20	22			RED
T1-21	CR54-2	14		(1) 42592-2 TERM.	BLUE
T1-22	C32+	14		(1) 31903 TERM.	BLUE/W
T1-23	CR54-4	14		(1) 42592-2 TERM.	BLUE

NOTE:
FOR COVER, SWITCH & POWER CORD ASSEMBLY SEE DWG NO. CP340M1700E

NOTE:
COVER ALL POTENTIOMETER ADJUSTING SCREWS WITH G.E. RTV #116 RED, PRIOR TO SHIPMENT.

CONSISTS OF:

SYM.	QTY.	PART NO.	DESCRIPTION
1A	1 AS REQ'D	DP340C0160E	H.V. PCB ASSEMBLY ≤ SN 500
		DP340C0160G	H.V. PCB ASSEMBLY > SN 500
		DP340C0150G	L.V. PCB ASSEMBLY > SN 500
1B	1	AP340M5700	TAG
1C	1	DP340M0400G	MAIN MOUNTING FRAME
1D	1	CP340M0500	P.C.B. MOUNTING PLATE
1E	1	08350	FASTENER 5" NAT. - DENNISON
1F	1	AP340M1100	FUSE LABEL
1G	1	BP340M1400	POWER CABLE
1H	1	AP332M1400	WARNING LABEL
1J	1	AP340M1500	ARROW DRAWING
1K	1	AP332M1600	PATENT LABEL
1L	1	AP340M5600	FUSE LABEL
1M	1	AP332M1000A	TERMINAL BLOCK LABEL
1N	1	115058-06	CAPACITOR BRKT. - SANGAMO
1P	5	PTS-2	SOCKET - U.I.D. ELECT. CORP.
1Q	5	43-03-9	INSULATOR - THERMALLOY
1R	1	CP340M2100	PERFORATED PLATE
1S	5	6903 NB	TRAN. COVER - THERMALLOY
1T	1	357-002	FUSE BLOCK - LITTELFUSE
1U	2	115058-05	CAPACITOR BRKT. - SANGAMO
1V	1	SR-6L-1	STRAIN RELIEF - HEYCO
1W	2	1445-06-X15E ZINC PLATE	MOUNTING POST - POSITRONIC
1X	4	511-101800-50 ZINC PLATE	LOCKNUT #10-32 - SHAKEPROOF
1Y	1	AP340M2300	FUSE WARNING LABEL
1Z	2	SCREW, SEMS PAN HD. #10-32	W/INTERNAL TOOTH L.W. ZINC PLATE - SHAKEPROOF
2A	2	14-50-5 ZINC PLATE	HEX. SPACER - ⅜ LG. - KEYSTONE
2B	7	511-061800-00 ZINC PLATE	LOCKNUT #6-32 - SHAKEPROOF
2C	6	511-041800-00 ZINC PLATE	LOCKNUT #4-40 - SHAKEPROOF
2D	6	SCREW, PAN HD. #4-40 ½	- ZINC PLATE
2E	12	SCREW, PAN HD. #6-32 x ⅜	- " "
2F	6	SCREW, PAN HD. #6-32 x ½	- " "
2G	1	SCREW, PAN HD. #6-32 x ¾	- " "
2H	4	SCREW, PAN HD. #10-32 x ½	- " "
2J	9	LOCKWASHER, INT. TOOTH #6	- " "
2K	12	LOCKWASHER, INT. TOOTH #10	- " "
2L	2	SCREW, BINDING HD #4-40 x ¾	- " "
2M	10	SCREW, PAN HD. SHEET METAL #6 x ½	- " "
2N	1	FLAT WASHER #6	- " "
2P	6	32561	TERMINAL - AMP
2Q	1 WHT, 1 BLK, 1 GRN	ALPHA #3057 OR EQUIV.	#16 AWG WIRE U.L. STYLE 1007, 300V, 80°C (3) PIECES - 35" LONG
Q5 Q4 Q2	4	2N5239	TRANSISTOR - RCA
Q7	1	2N6383	TRANSISTOR - RCA
R64	1	HLM-10	RESISTOR (12Ω, 10W, 10%) - DALE
R35	1	RCR-32	RESISTOR (39 KΩ, 1W, 10%) - A.B.
R63	1	RCR-07	RESISTOR (8.5 KΩ, ¼W, 10%) - A.B.
CR54	1	KBH25005	BRIDGE - G.I.
F5	1	312.005	FUSE N.B. 5AMP - LITTLEFUSE
F7	1	312.003	FUSE, N.B. 3AMP - LITTLEFUSE
C30	1	500-6520-02	CAP. (1200 mfd., 200V) - SANGAMO
C31	1	36DX251F200AA2A	CAP. (250 mfd., 200V) - SPRAGUE
C32	1	10828U0202BK2B	CAP. (22000 mfd., 20V) - SANGAMO
J1	1	REF.	OUTPUT PRINTED CIRCUIT Bd.
T1	1 AS REQ'D	CP340M0400H	TRANSFORMER ASSEM. ≤ SN 500
		CP340M2400K	TRANSFORMER ASSEM. > SN 500
	1 AS REQ'D	DP340M1900A	WIRING HARNESS ≤ SN 500
		DP340M1900B	WIRING HARNESS > SN 500
	1	42599-2	TERMINAL - AMP
	1	31903	TERMINAL - AMP
	2	42332-2	TERMINAL - AMP
	7	31889	TERMINAL - AMP
	SUFF. AMOUNT		G.E. RTV #116 RED
2R	5	TYB-23M	CABLE TIE - THOMAS BETTS
R65	1	V10M7T	RESISTOR (7Ω 10W 10%) - CLAROSTAT

WIRES TO BE #18 AWG, U.L. STYLE #1007 ~ 300 V ~ 80°C (RED, YELLOW & GRAY)

2S	1	AP340M2200	FUSE LABEL

CONT'D.

G	ECO#10	11-7-74	EP
F	ECO #8 + #9		
REF. ASSEMBLY			
E	REVISED PER ECO#6	11-7-74	MEG.
D	ECO.5	10-18-74	WB
C	ECO 2,44	10-11-74	WB
B	REVISE W-17 LENGTH & J1-8 COLOR	9/19/74	MEG.
A	REVISED	9-17-74	
NO	REVISIONS	DATE	BY

TOLERANCES: ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

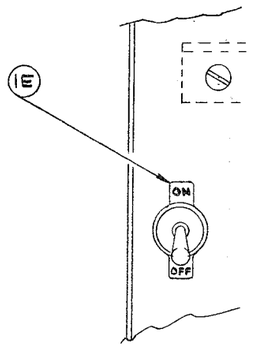
MATERIAL

DIGIVUE®
DISPLAY/MEMORY UNITS
OWENS-ILLINOIS 12/17/73

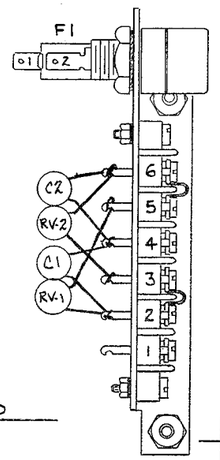
TITLE: FINAL ASSEM. LAYOUT

DRAWN	CHECKED	APPROVED	DATE
MEG.			

SCALE: 1/1 DRAWING NO. DP340M1300E

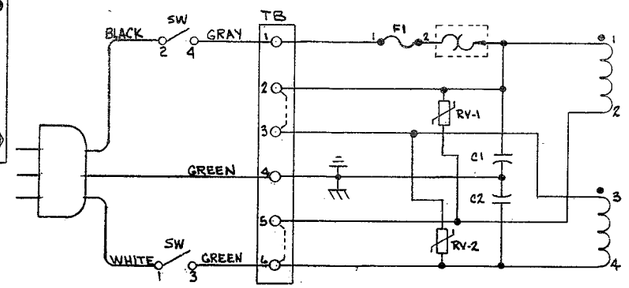


VIEW B



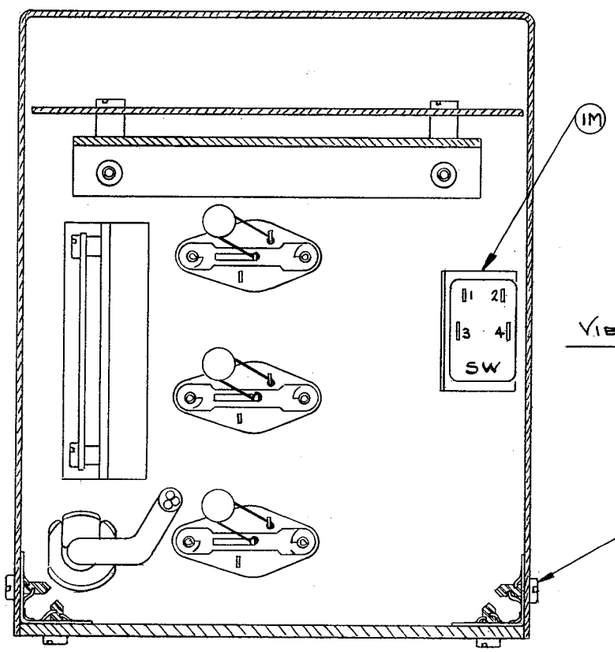
WIRING LIST

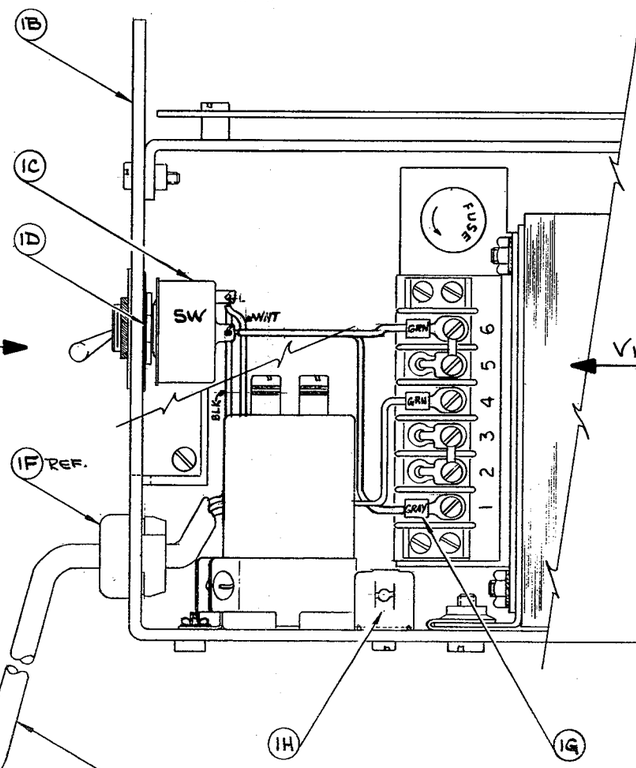
TERM.	POINTS	GAGE	LENGTH	REMARKS	COLOR
TB-6	SW-3	18	8"	(1) 31879 TERM.	GREEN
PC(BLK)	SW-2				BLACK
PC(WHT)	SW-1				WHITE
TB-1	SW-4	18	8"	(1) 31879 TERM.	GRAY
PC (GRN)	TB-4			(1) 31879 TERM.	



CONSISTS OF:

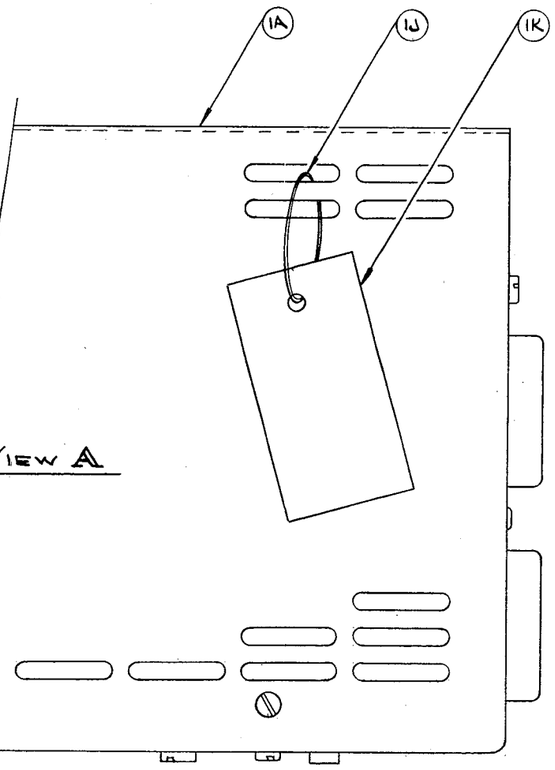
SYM.	QTY.	PART NO.	DESCRIPTION
1A	1	CP340M0900A	COVER
1B	1	BP340M1300P	POWER SUPPLY ASSEMBLY
1C	1	8370K8	SWITCH - CUTLER HAMMER
1D	1	16-886	LOCKWASHER - CUTLER HAMMER
1E	1	30-5632-4	IND. PLATE - CUTLER HAMMER
1F	1	SR-6L-1	STRAIN RELIEF - HEYCO(REF)
1G	3	31879	TERMINAL - AMP
1H	4	C6083-8A-67	ANGLE BRKT. - TINNERMAN
1J	1	08350	FASTENER-5" NAT. - DENNISON
1K	1	AP340M5700	TAG
1L	8	SCREW, PAN HD. SHEET METAL #8x3/8-ZINC PLATE	
PC	1	17405	POWER CORD - BELDEN
1M	1	BP340M2800	INSULATOR (FISHPAPER)





VIEW B

VIEW A



VIEW A

NOTE:
SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

NOTE:
ZINC PLATING PER ZINC DICHROMATE SPEC 210M0200A TYPE # CLASS 2.

Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document.

Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.

NO	REVISIONS	DATE	BY
REF ASSEMBLY			
E	REVISED PER ECO# 41&42	5/20/76	MRG
D	REVISED 1B & 1L, ECO#2326	4/8/75	MRG
C	ECO#21	3/9/75	FP
B	ECO#17		
A	REVISED PER PRE PRODUCTION DWG	12/4/74	FP

TOLERANCES: ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL

DIGIVUE®
DISPLAY/MEMORY UNITS
OWENS-ILLINOIS 7/10/74

TITLE: SWITCH & COVER ASSEMBLY

DRAWN	CHECKED	APPROVED	DATE
M.R.G.	FP	KCM	7-16-74

SCALE 1:1 DRAWING NO. CP340M1700E

MM608

DIGIVUE®
MAINTENANCE MANUAL 512-60

DISPLAY D141

MM608

DIGIVUE®
MAINTENANCE MANUAL 512-60

DISPLAY D141

Owens-Illinois, Inc.
Electro/Optical Display Business Operations
Post Office Box 1035
Toledo, Ohio 43666
(419) 242-6543

Owens-Illinois, International S.A.
50, route des Acacias
1227 Carouge-Geneva, Switzerland
(022) 43 62 00

OWENS-ILLINOIS

$5.00
G

DIGIVUE® display/memory units are designed and produced for OEM (Original Equipment Manufacturer) applications, and as such are intended to be mounted in the purchaser's equipment or product. It is the responsibility of the purchaser to insure, as necessary, that the display unit and power pack are installed and used in accordance with Underwriter's Laboratories, government, or other applicable rules and regulations governing their end use (such as UL 114, NFPA pamphlet 75). Certain items which may be supplied with the display unit or power pack (e.g., cover, power switch, AC cord, etc.) are for the convenience of the purchaser only and are not intended to suggest possible uses for the display unit or power pack. Nor do they indicate that the display unit or power pack may be used as an end product as received by the purchaser without being incorporated into his equipment or in some way modified to meet the appropriate rules and regulations governing the end use of the display system.

Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document.

CONTENTS

ILLUSTRATIONS

1.0 INTRODUCTION

This manual is to be used in conjunction with DIGIVUE® User Manual 512-60, UM607. Together, these manuals provide detailed information relating to the installation, operation, and maintenance of the model 512-60 DIGIVUE® display/memory unit, D141.

The emphasis in this manual is upon providing a thorough understanding of the electronic circuits used in the display and their interrelationships to each other; and upon trouble-shooting and repair procedures for the system. It is suggested that before any action is taken to correct what appears to be a faulty display, the repairman become thoroughly familiar with the material contained in this manual and UM607. In doing so, he will not only save time in locating the fault, but will also become familiar with the terminology used in plasma display technology and will have a common point with others from which to discuss and inquire about the system.

2.0 DISPLAY CIRCUIT SUBGROUPS AND INTERCONNECTIONS

2.1 Display Panel

The display panel used in the model 512-60 DIGIVUE® display/memory unit is a 512 line by 512 line dot matrix device. Information is displayed as a series of discrete bi-stable gas discharges.

Basically, the display panel consists of two quarter inch thick glass plates (see figure 2.1). Each plate, or substrate, has parallel conductive electrodes deposited upon one surface with an overcoating of a clear dielectric material. The two plates are assembled with their electrodes at right angles and their dielectric surfaces facing, but separated by a small gap. The assembled plates are cemented together at their perimeter and the gap is filled with a neon based gas mixture; then permanently sealed. The display panel is completed by bonding flexible ribbon cables to the exposed ends of the electrodes (ribbon cables are used to connect the display panel to the drive electronics).

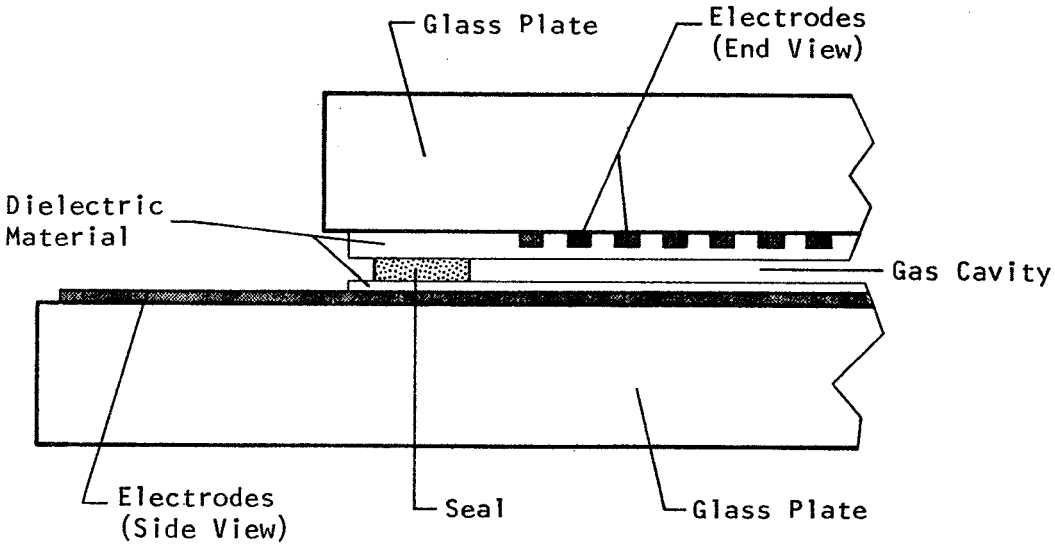


Figure 2.1 - Display Panel Cross Section

The display panel contains three types of electrodes (see figure 2.2): those which make up the 512 line x 512 line display matrix or ACTIVE AREA, the display matrix conditioning electrodes, and the border electrodes. Only the active area electrodes are used to display information; all others serve only to produce conditions within the display panel which are conducive to the reliable formation of gas discharges.

2.2 Sustainer Circuitry

The sustainer circuits supply the basic AC waveforms necessary to maintain gas discharges in the display panel AFTER they have been started. Two types of sustainers are employed: one supplying waveforms to the active area and display matrix conditioning electrodes, called simply the SUSTAINER; and another supplying special waveforms to the border electrodes, called the BORDER SUSTAINER.

2.3 Address Circuitry

The ADDRESS CIRCUITRY is used to modify the basic sustainer waveforms to start or stop (WRITE or ERASE) individual gas discharges in the display active area. The address circuitry consists of the following subcircuits:

2.3.1 Resistor Pulsers

The RESISTOR PULSERS produce high voltage pulses (ADDRESS PULSES) which, when added to the sustainer waveforms at the appropriate times in the display cycle, cause gas discharges to be written or erased in the active area.

2.3.2 Diode Switch Matrix Circuits

The DIODE SWITCH MATRIX CIRCUITS are used as part of the scheme to multiplex address pulses onto the active area electrodes. They also provide part of a bi-directional current path between the display panel and the sustainers for the capacitive displacement currents of the plasma panel.

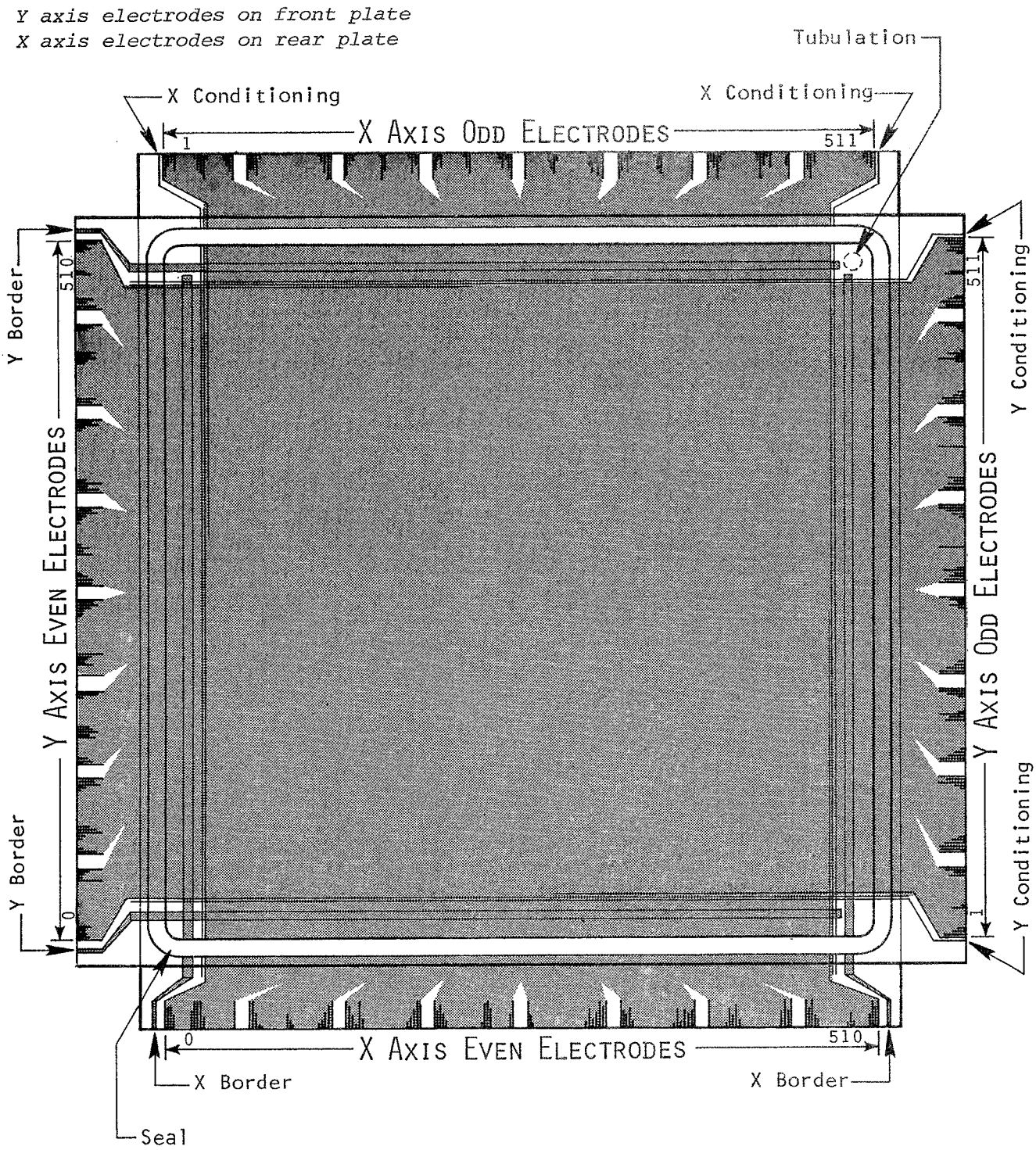


Figure 2.2 - Display Panel Electrode Locations (Front View)

2.3.3 Keyers

The KEYER circuits are used to help shape the address pulses for optimum display operation.

2.3.4 Diode/Resistor Matrix

The DIODE/RESISTOR MATRIX serves as a junction between the sustainers, resistor pulsers, and diode switch matrix circuits; and the active area electrodes. It is also used in conjunction with the resistor pulser and diode switch matrix circuits to multiplex address pulses onto the active area electrodes.

2.4 Control/Interface Logic

The CONTROL INTERFACE LOGIC buffers and decodes all incoming interface signals and automatically generates other signals to select and control all phases of display operation.

2.5 Circuit Interconnections

The display panel electrodes and their associated circuitry are divided into two main groups: the X and Y axes (the vertical and horizontal electrodes respectively). Each display axis has its own separate sustainer, border sustainer, and address circuitry connected to it. Since the X and Y axis circuits are similar, the following explanation of the X circuits (illustrated in figure 2.3) can also be applied, with minor modification, to the Y circuits. (Important differences between the X and Y circuits will be noted in the text.)

The X axis active area electrodes are numbered from 0 through 511; left to right when viewed from the front of the display. The even numbered electrodes exit from the bottom edge of the display panel; the odd numbered ones from the top. Each active area electrode has two diodes (D1 and D2)* and one resistor (R1)* connected to it. Collectively, these diodes and resistors comprise the X axis diode/resistor matrix.

All D1 diodes in the X axis are bussed together and connected to the X axis sustainer. (Note that the X display matrix conditioning electrodes are also numbered to the X axis sustainer.)

* *These component designations are for this explanation only and do not reflect the actual designations used in the circuitry.*

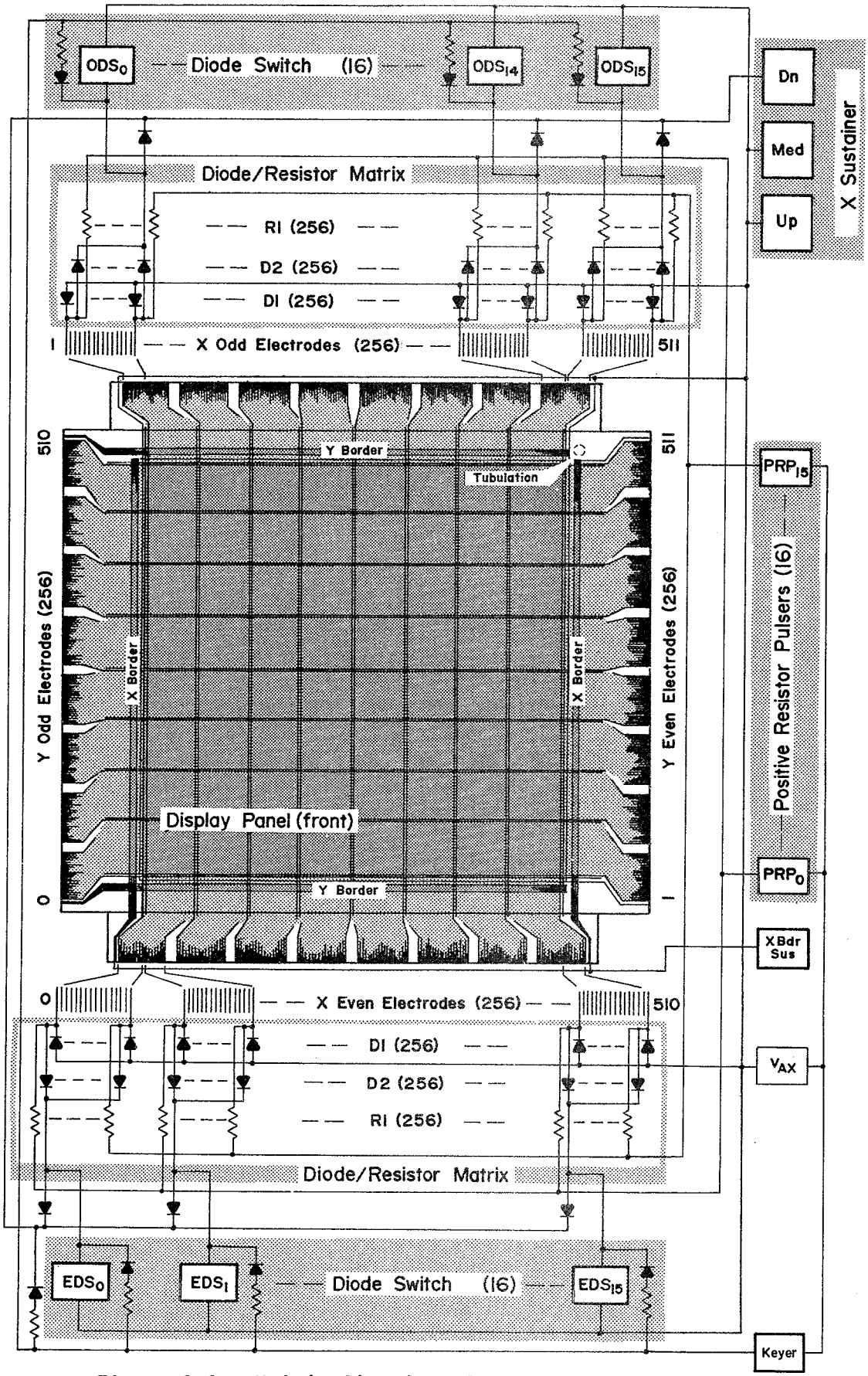


Figure 2.3 - X Axis Circuitry Interconnection Diagram

To aid in explaining the connections to the D2 diodes and R1 resistors, the even numbered X axis active area electrodes, and likewise the odd electrodes, may be further subdivided into 16 groups of 16 electrodes each. For this explanation only, the electrodes within each group are numbered 0' through 15'.

All of the D2 diodes from a given 16-electrode group are bussed together and connected to one of the 16 outputs from the appropriate diode switch matrix circuit. (There are two diode switch matrix circuits in the X axis; one associated with the even electrodes, the other with the odd.)

The R1 resistors connected to the 0' electrode from both the even and odd 16-electrode groups are bussed together and connected to the output of one of the 16 resistor pulser circuits in the axis. The R1 resistors from the 1', 2'... through 15' electrodes are connected in a similar manner to the outputs of the remaining resistor pulsers.

All 16 of the resistor pulser circuits in the X axis are connected to a common voltage source, V_{AX}, which is referenced to the X sustainer waveform. This voltage will be switched by the resistor pulser circuits to produce address pulses. (The Y axis resistor pulsers are connected to a different voltage source, V_{AY}, which is referenced to the Y sustainer waveform.)

The output of the single X keyer circuit is connected through isolation diodes to each output of both the diode switch matrix circuits and to part of the X sustainer. The keyer takes its power from the V_{AX} voltage source. (The Y axis keyer is connected to the V_{AY} voltage source.)

Both sets of X axis border electrodes are connected directly to the output of the single X border sustainer circuit.

3.0 DISPLAY OPERATION

3.1 Normal Sustain (Display Idle)

Figure 3.1 illustrates a simplified schematic of the circuitry connected to one active area electrode in the X axis. During a normal sustain operation (no write, erase, or bulk erase operations being performed) only the sustainer, diode switch matrix circuits, and diode/resistor matrix enter into the maintenance of gas discharges in the display panel.

The X sustainer impresses the waveform shown in figure 3.2a upon the electrode. This waveform is generated by turning the three sustainer output transistors on and off in response to specially timed logic level signals. These signals are automatically generated by the control/interface logic.

The three sustainer output transistors are referred to as: the "pull-up" (XUS) which applies the full potential of the sustainer voltage supply (V_{SS}) to the electrode; the "pull-down" (XDS) which switches the electrode to sustainer ground; and the "pull-medium" (XM) which applies an intermediate voltage (V_{MX}) to the electrode. The three output transistors are connected to the electrode through diodes D1 amd D2 of the diode/resistor matrix.

Figure 3.3 illustrates the simplified schematic of the circuitry connected to one active area electrode in the Y axis. The circuit is similar to that of the X axis in (figure 3.1), the main difference being the manner in which the sustainer circuits are connected to the diode/resistor matrix.

The Y sustainer circuit generates the waveform shown in figure 3.2b and impresses it upon the Y active area electrode. This is done in essentially the same manner as in the X axis.

The sustainer waveforms impressed upon the X and Y active area electrodes result in the composite sustainer waveform, shown in figure 3.2c, being present across the gas at each point in the display panel where the X and Y active area electrodes intersect. The peak potential (V_{SS}) of the composite sustainer waveform is adjusted at the power source so that it does not exceed the breakdown voltage of the gas.

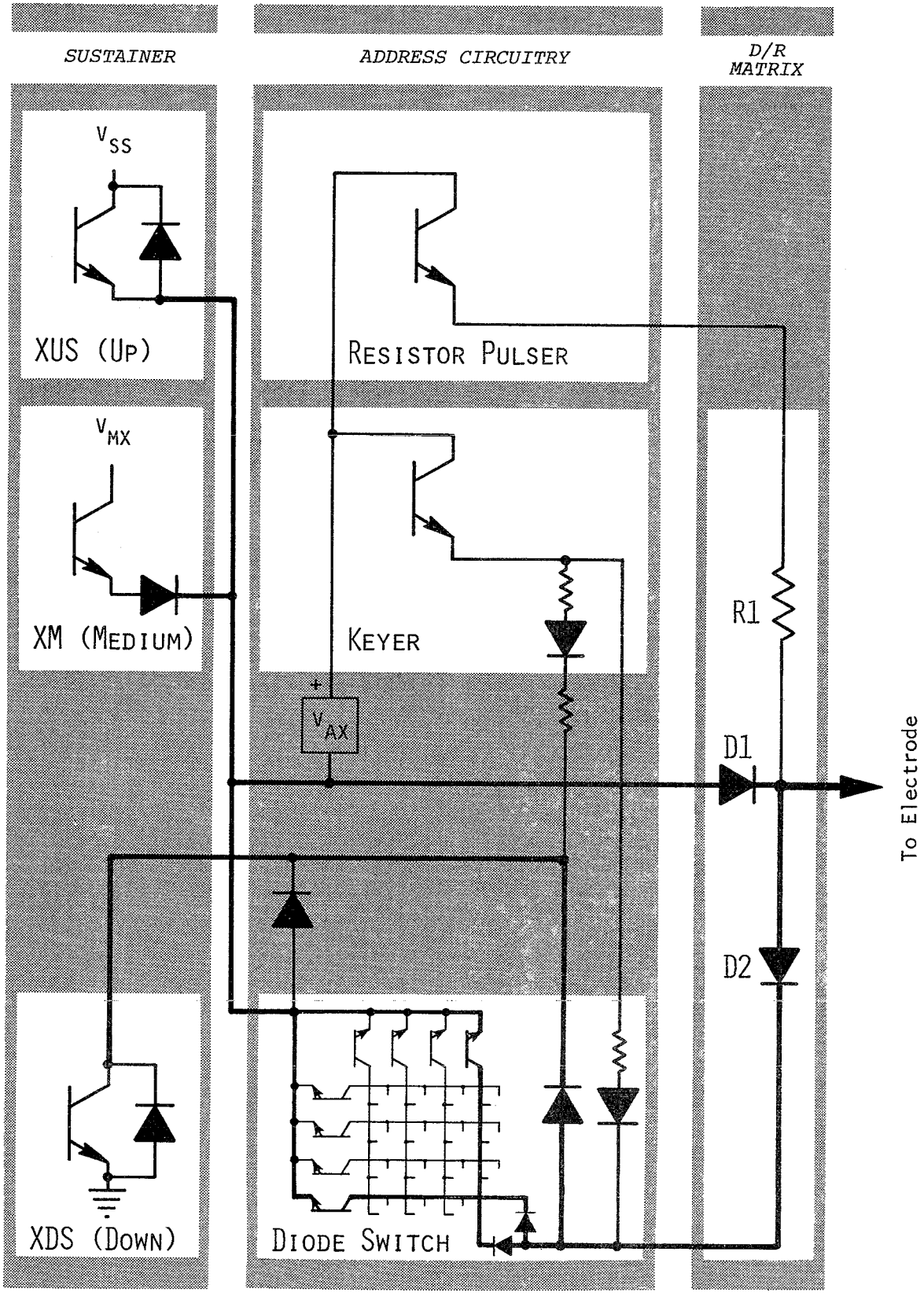


Figure 3.1 - Simplified X Axis Display Circuitry

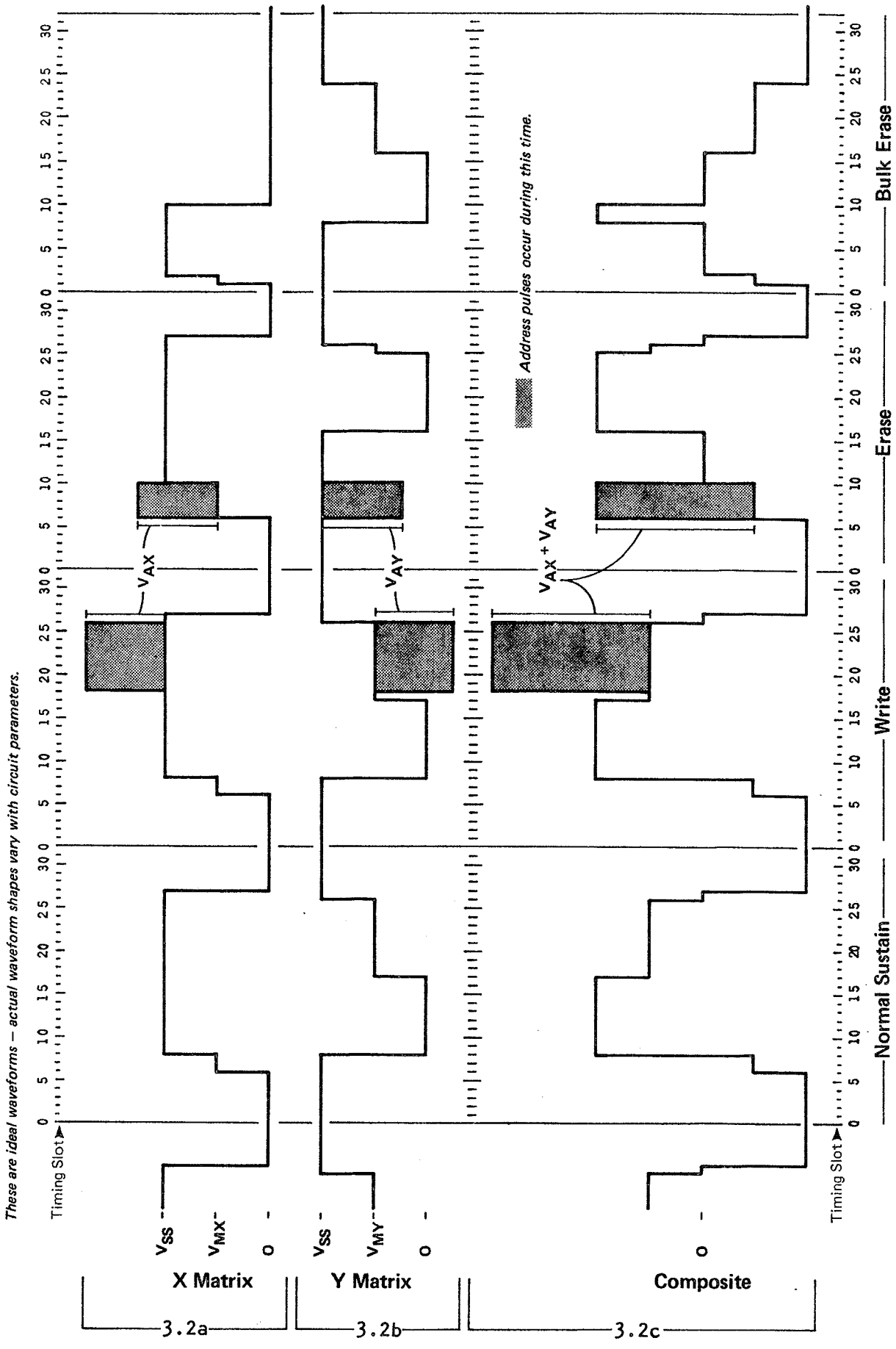


Figure 3.2 - Display Matrix Sustainer Waveforms

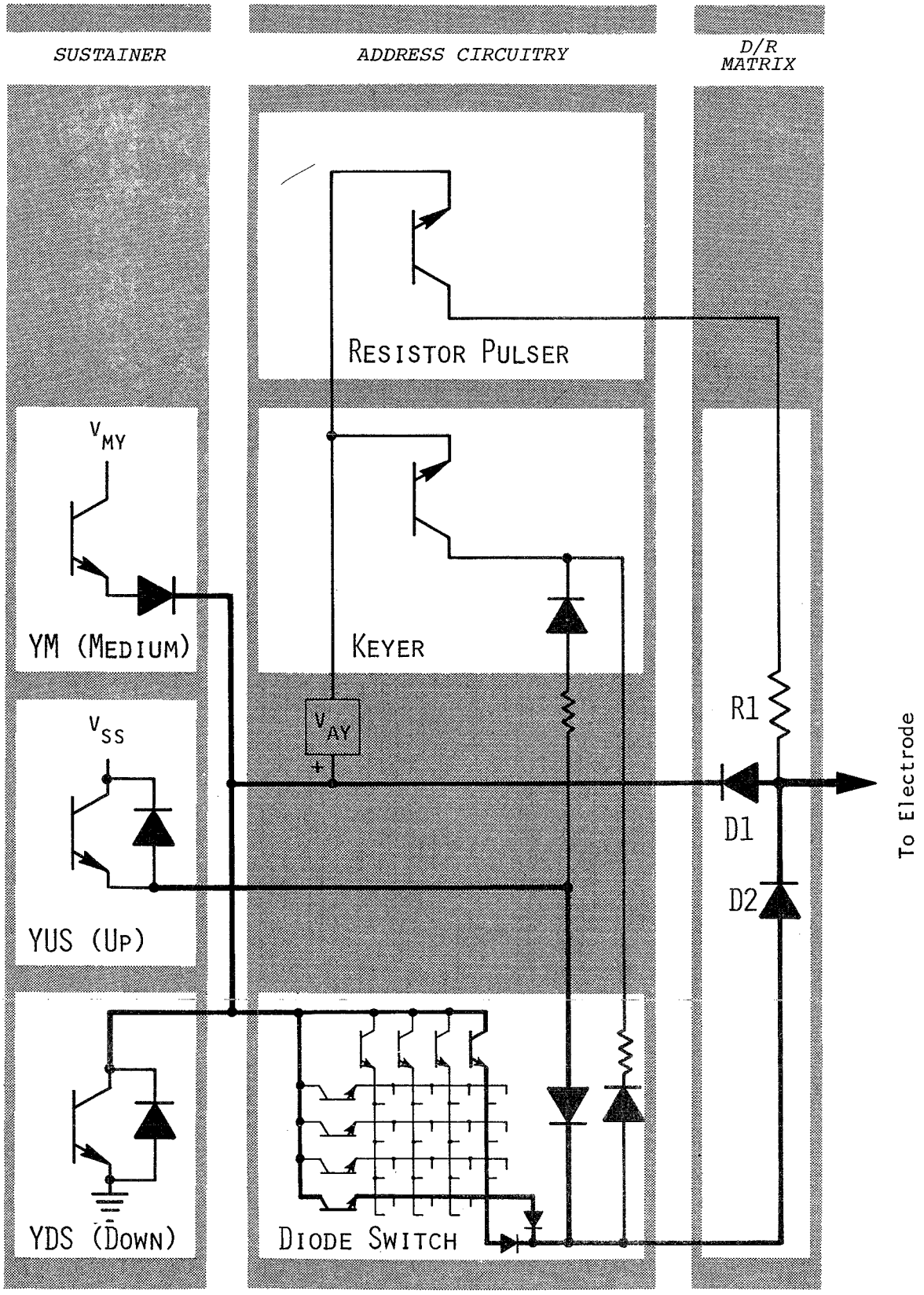


Figure 3.3 - Simplified Y Axis Display Circuitry

The composite sustainer waveform, therefore, cannot by itself initiate a gas discharge. (The manner in which gas discharges are started and how they are maintained by the composite sustainer waveform will be explained in the next section.)

There are times during the normal sustain cycle (and all other display cycles as well) that it is necessary to have a bi-directional current path between the display panel electrodes and the sustainer output transistors. Part of this path is through the D1 diodes. Current flowing in the opposite direction, however, must pass through the D2 diodes and the diode switch matrix. It is necessary to turn on the diode switch matrix drive transistors in order to complete this half of the current path. All of these transistors are turned on simultaneously for brief periods, as required during each display cycle.

3.2 Write Operation

The interaction of all parts of the circuits illustrated in figures 3.1 and 3.3 is required to write a gas discharge at the point in the active area where an X and a Y electrode intersect.

At the proper time during the display cycle, the X resistor pulser output transistor is turned on for approximately 5 microseconds in response to signals produced by the control/interface logic. At the same time the control/interface logic turns on all the diode switch matrix drive transistors EXCEPT the two that are associated with the matrix diodes connected to the electrode to be addressed. The full potential of the X resistor pulser voltage supply (V_{AX}), which is referenced to the sustainer waveform, is applied to the R1 resistor in the form of a positive address pulse. The D1 diode and the open diode switch matrix output prevent the write address pulse from being dissipated across the R1 resistor by blocking the current path back to the reference (negative) side of the V_{AX} supply. The address pulse is forced to appear on the electrode and, in combination with the sustainer waveform, results in the modified X axis sustainer waveform depicted in the WRITE cycle of figure 3.2a.

(The address pulse is also applied to other R1 resistors which are connected to electrodes that are not to be addressed. Since current paths exist from these R1 resistors back to the resistor pulser voltage source, the address pulse will be dissipated across the R1

resistors, and will not appear on the nonaddressed electrodes. The current paths mentioned are through the diode switch matrix diodes and the remaining drive transistors that are turned on in coincidence with the address pulse.)

The X Keyer circuit is turned on near the end of the resistor pulser signal for approximately 0.6 microseconds, providing an additional source of current to the resistor pulser output. This results in improved display operation over a broader range of sustainer and resistor pulser voltage settings.

The Y axis circuits operate in essentially the same way as described in the foregoing paragraphs to produce the modified Y sustainer waveform (figure 3.2b, WRITE cycle) on the Y active area electrode. The address pulse produced by the Y address circuits is negative with respect to the Y sustainer waveform.

At the point where the addressed X and Y electrodes intersect, the modified composite waveform shown in the WRITE cycle of figure 3.2c will be impressed across the gas. The amplitude of the modified composite waveform exceeds the breakdown voltage of the gas so that a discharge occurs.

As the discharge initiated by the address pulse progresses, a charge, called WALL CHARGE or WALL VOLTAGE, collects on the surface of the display panel dielectric layer at the point of the discharge. The wall charge, which opposes the potential that is present across the gas, continues to increase until the net potential across the gas is zero and the discharge ceases.

As the composite sustainer waveform reverses polarity, the wall charge remains to act as a bias voltage. The polarities of the reversed composite sustainer waveform and the remaining wall charge are the same so that they add and together exceed the breakdown voltage of the gas. Another discharge begins, without the aid of an address pulse, and the wall charge again collects as previously described. This process of reversing the composite

sustainer waveform and the formation of wall charge maintains the discharge through succeeding display cycles until the discharge is terminated by either an erase or bulk erase operation. The ability of the DIGIVUE® display/memory unit to indefinitely retain information in the form of gas discharges is referred to as INHERENT MEMORY.

3.3 Erase Operation

Gas discharges in the active area are erased in much the same way that they are written. The circuits in figures 3.1 and 3.3 produce address pulses as when writing, but at a time in the display cycle so that the modified X, Y, and composite sustainer ERASE waveforms of figure 3.2 are produced.

The wall charge produced by the discharge to be erased, together with the erase address pulse, cause a discharge sequence to occur at a time in the display cycle such that the resulting wall charge is at or near the zero level of the composite sustainer waveform. Since the amplitude of the composite sustainer waveform, without the wall charge to act as a bias voltage, does not exceed the breakdown voltage of the gas; the discharge sequence is interrupted and the discharge stops.

3.4 Nonaddressed Points During Write and Erase Operations

The foregoing descriptions of the write and erase operations were concerned with just the gas discharge site located at the intersection of the addressed X and Y electrodes. As explained, this is the only point in the active area at which the composite sustainer waveform of figure 3.2c will be impressed across the gas to write or erase a discharge.

The points where addressed and nonaddressed electrodes intersect will also have a modified composite sustainer waveform impressed on the gas which is similar to the one in figure 3.2c. The amplitude of the address pulse will be one half of $V_{AX} + V_{AY}$. This is insufficient to cause a change in state of the intersection points involved.

During write and erase operations, the points which are not associated with either the X or Y addressed electrodes will have the same composite sustainer waveform impressed on the gas as during a normal sustain cycle.

3.5 Bulk Erase Operation

The bulk erase operation uses specially shaped sustainer waveforms, without the aid of address pulses, to erase all the discharges present in the active area of the display panel.

During a bulk erase operation, the control/interface logic supplies specially timed signals to all the sustainer circuits in the display system, producing the

bulk erase sustainer waveforms illustrated in figure 3.2. The bulk erase composite sustainer waveform is present across the gas at every electrode intersection in the active area. The timing of this waveform is such that the discharges which result are of a shorter duration than normal. The wall charge resulting from these short duration discharges does not have sufficient time to collect to a level which is high enough to produce a continuing discharge sequence, and all active area discharges are extinguished.

3.6 Border Discharges

Border discharges are maintained at all times while the display is in operation to provide conditions conducive to the formation of gas discharges within the active area.

Each of the two border sustainer circuits, which supply the waveforms to the X and Y axis border electrodes, has two output transistors, (as opposed to three in the active area sustainers): A "pull-up" (XUB, YUB) which supplies the full border sustainer voltage (V_{SS} + V_{SB}) to the border electrodes; and a "pull-down" (XDB, YDB) which connects the border electrodes to sustainer ground.

The waveforms produced by the border sustainers are illustrated in figure 3.4. The composite border sustainer waveforms shown are the result of the waveforms on the border electrodes in combination with the sustainer waveforms present on the intersected active area electrodes.

When the display is first turned on, it is necessary to increase the V_{SB} supply level until the amplitude of the border composite sustainer waveforms exceed the gas breakdown voltage. This starts the border discharges, after which V_{SB} is lowered to its normal operation level. Border discharges are then maintained through the combination of the border composite waveforms and wall charge.

Border discharges are maintained during all display cycles. During a bulk erase operation, specially timed sustainer waveforms are used to prevent the erasure of the border discharges (see figure 3.4).

3.7 Display Matrix Conditioning Electrodes

The voltage level of the sustainer waveform appearing on any given active area electrode is influenced to some extent by the capacitative coupling of the signals

These are ideal waveforms — actual waveform shapes vary with circuit parameters.

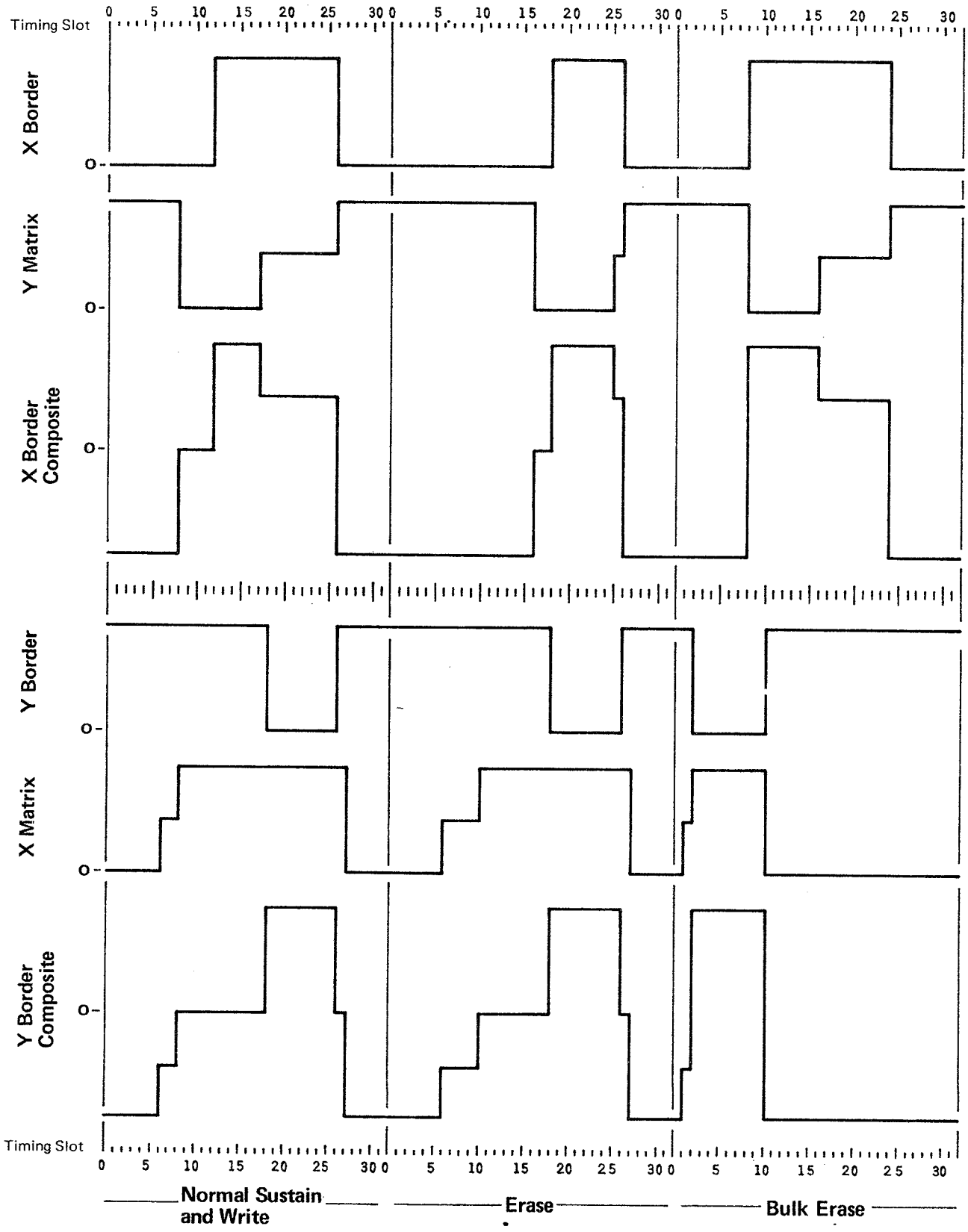


Figure 3.4 - Border Sustainer Waveforms

present on its neighboring electrodes. The display matrix conditioning electrodes, which are connected to the sustainers, are provided so that the signal coupling to the first and last addressable active area electrodes will be the same as for all others. This improves the reliability with which gas discharges can be written or erased on the edge electrodes.

3.8 Address Decoding

The signals (bits) which make up the X and Y address words are decoded in the same manner in each axis to select the appropriate address circuits, and multiplex the address pulse onto the electrodes. The following explanation of this decoding and selection process will apply to both axes (see figure 3.5).

Bits 0 and 5 through 8 from the address word are used to select the appropriate diode switch matrix output. The diode switch matrix circuit associated with either the odd or even electrodes is selected by bit 0, and in turn one of its diode matrix outputs is selected by bits 5 through 8. As a result any one of the 16 electrodes connected to the selected diode switch matrix output can potentially receive the address pulse.

One of the 16 resistor pulser circuits in the axis is selected by bits 1 through 4. The selected resistor pulser circuit applies its address pulse to one electrode from each 16-electrode group.

The one electrode which is common to both the selected diode switch matrix output and the selected resistor pulser circuit will receive the address pulse. Those electrodes associated with the selected resistor pulser and a nonselected diode switch matrix output will have the address pulse dissipated across their R1 resistor as explained in section 3.2. The electrodes associated with the selected diode switch matrix output and a nonselected resistor pulser will not receive an address pulse since none is produced. The remaining electrodes are unaffected by the write or erase operation.

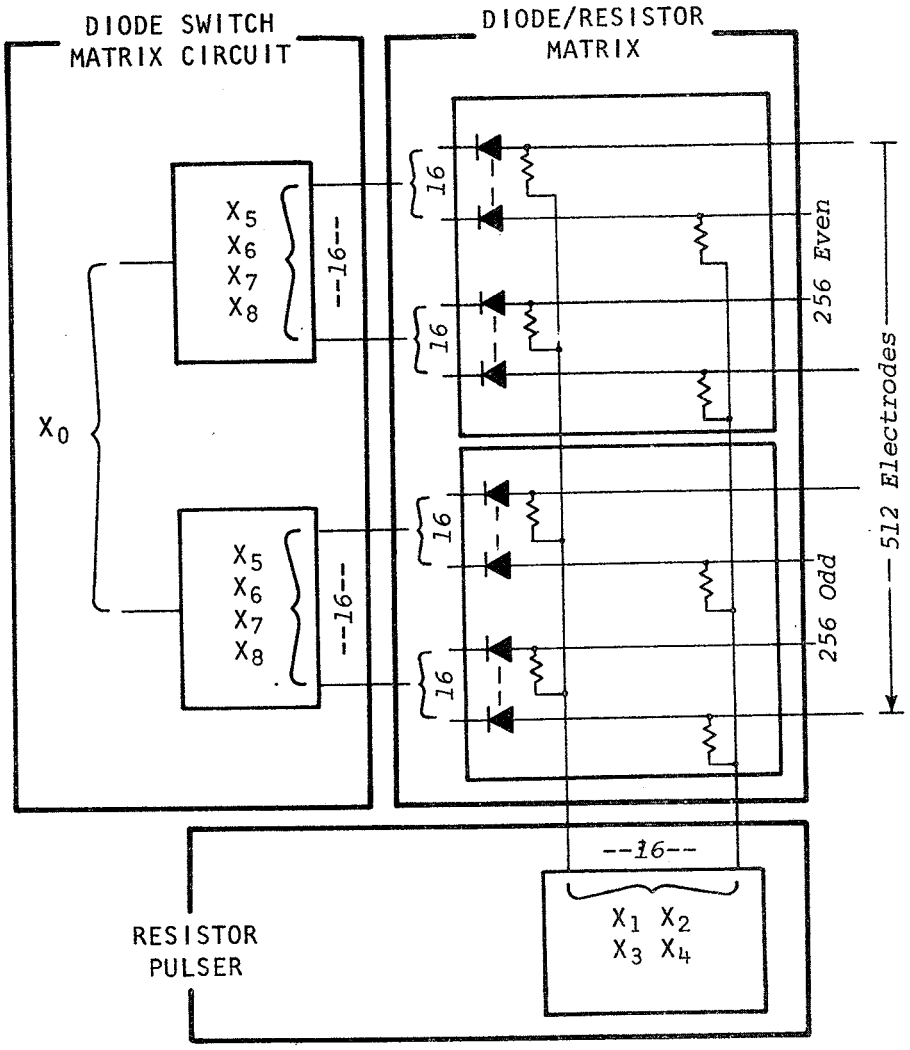


Figure 3.5 - Address Word Decoding and Circuit Selection

4.0 SYSTEM BOARD DESCRIPTIONS

4.1 100 Board

The 100 board contains most of the control/interface logic in the display system. The following description of the circuits on this board should be accompanied by drawing DD-340E2000.

4.1.1 Address and Control Signals

Each of the 18 signals from the interface signal connector (P100) which comprise the X and Y address words, $X_0 \ldots X_8$ and $Y_0 \ldots Y_8$, is terminated by a 1000 ohm resistor to V_{CC} (+5VDC) and then connected to a single buffer logic element. After buffering, most of these signals leave the 100 board for distribution to other circuits in the display system. Some of them are also distributed in their inverted form.

Bit X_0 of the X address word is processed by one half of a 2-4 line decoder (U20-74156) to produce two signals, "X even" and "X odd". These signals are used to select the diode switch matrix circuit associated with either the odd or even X electrodes during write and erase operations. Bit Y_0 is processed by the remaining half of U20 to produce similar signals for the Y axis.

The duration of the diode switch matrix circuit selection signals described above is determined by a strobe signal connected to pins 2 and 14 of U20. The purpose of the strobe signal and the method of its generation will be explained later.

A second 2-4 line decoder (U16-74156), connected in a similar configuration and using the same strobe signal as U20, is used to process bits X_4 and Y_4 into signals used in the selection of the resistor pulser circuits during write and erase operations.

4.1.2 Master Clock

System timing is governed by an oscillator (U12-74122) whose frequency is determined by the RC time constant of C14, R5, and R6; and adjusted to 1.6 megahertz (625 nanosecond period).

WARNING

Do not change the output frequency of the master clock, U12.

4.1.3 Display Operation Selection

The primary CONTROL signals, C_0 and C_1, from pins 14 and 15 of the interface signal connector (P100) are terminated by 1000 ohm resistors to V_{CC} (+5VDC). The three alternate control signals; Write, Erase, and Bulk Erase (pins 5,7, and 6 of P100); are likewise terminated and are then decoded by U22 (7400) and U32 (7412) to produce two signals which are compatible with the C_0 and C_1 signals. Each decoded signal is connected along with its corresponding C_0 or C_1 signal to the input of a noninverting buffer (U14 - 7417).

The two buffered control signals are connected to the inputs of edge triggered flip-flops (U6 - 7474). Near the end of each display cycle, a LO going LOAD signal at pins 3 and 11 of U6 causes the control signals to be transferred to the inverted outputs of U6. The signals are transferred to the outputs of U6 at the positive edge of LOAD. The inverted and latched control signals are then decoded by a 2-4 line decoder (U5 - 74155) into four signals: $\overline{B}$, $\overline{W}$, $\overline{E}$, and $\overline{S}$. These are LO going signals which are used to enable or inhibit other logic circuits as appropriate for bulk erase, write, erase, or normal sustain display cycles respectively.

4.1.4 System Program ROMs

The output pulse train from U12 pin 8 is fed to the input of two cascaded 4-bit binary counters (U10 and U11-74161). The first five stages of the counters are used to supply the input address for 5 system program ROMs (U17, U18, U19, U33 and U34). Since each ROM contains 32 8-bit words in its program, and the count capacity of the five ROM address counter stages is also 32, the time that each word will be present at the ROM output will correspond to the period of the ROM address counter input (pin 2 of U10 and U11), or 625 nanoseconds. This causes the complete ROM program to be scanned and repeated every 20 microseconds,

and forms the basis for the 20 microsecond (50Khz) display cycle period.

The display cycle is divided into 32 "time slots", numbered 0 through 31, with each time slot corresponding to the time a particular word is present at the program ROM outputs. The timing charts and waveforms included in this manual are divided into increments which correspond to these time slots.

The five program ROMs are enabled in 3 combinations to control the display during 3 main phases of operation. One phase includes the normal sustain and write operations, another the erase operation, and the remaining one the bulk erase operation.

Rom U18 is enabled by the $\bar{E}$ signal from pin 6 of U5. It is therefore enabled during just the erase cycle.

The $\bar{W}$ and $\bar{S}$ signals from U5 are combined to produce an enable signal for ROM U34. Pin 15 of U34 is held LO during both write and normal sustain cycles.

ROMs U19 and U17 are enabled by the $\bar{B}$ signal from pin 4 of U5 and are therefore enabled during only the bulk erase cycle.

The inverted $\bar{B}$ signal from U5 enables ROM U33 during all except the bulk erase cycle.

The five outputs from the ROM address counters are connected directly to the inputs of ROM U18, U19, and U34 so the program words from these ROMs correspond to the display cycle timing slots as previously described. However, only the four highest order outputs from the ROM address counters are used to provide the addresses for ROMs U33 and U17. These address signals are connected to the four lowest order inputs of the U33 and U17 ROMs. The remaining input to each of these ROMs (the most significant bit) is connected to a signal which does not change during a given display cycle. Therefore, only the first or second half of the ROM program is read out during a cycle, as determined by the HI or LO state of the MSB address signal. Each word in the program is then present at the ROM output for two timing slots.

The outputs from each program ROM are connected in parallel with corresponding outputs from other ROMs so that the circuits to which they are connected will be con-

trolled by the proper ROM during a given display cycle. Most of the ROM output signals pass through noninverting buffers for increased drive capability before being distributed to other circuits in the display system.

4.1.5 LOAD Signal Generation

LOAD is a LO going pulse which occurs during timing slots 30 and 31 of each display cycle (except during a BULK cycle when it occurs just during timing slot 31). It is used to transfer data from the control signals to the input of the display operation decoder (U5).

4.1.6 SYNC Output Signal Generation

SYNC is a HI going, 50KHz system clock. It is derived from the 50KHz squarewave output of the ROM address counters (pin 14 of U11), and from signals produced at pin 1 of ROMs U18, U34, and U19.

The LO going output signals from pin 1 of ROMs U18, U34, and U19 are wire-NOR connected. The resulting signal, which consists of combinations of LO going pulses that vary with the display cycle, is inverted and connected to pin 10 of U3 (7400).

The 50KHz squarewave signal from pin 14 of U11 is double inverted and connected to pin 9 of U3. This signal is HI during the last half of each display cycle.

The resulting LO going pulse at pin 8 of U3 is connected to the input of an open-collector inverter/buffer (pin 1, U23 - 7416). The final SYNC output from pin 2 of U23 is connected through a 1000 ohm resistor to V_{CC} (+5VDC) and then to pin 3 of the interface signal connector (P100). (See section 5.15 for SYNC waveform timing.)

4.1.7 STATUS Output Signal Generation

STATUS is a LO going output signal used as a busy-done indicator. It is derived from the 50KHz and 100KHz squarewave outputs of the ROM address counters (pin 14 of U11 and pin 11 of U10, respectively), the $\overline{S}$ signal from the display operation decoder (pin 7 of U5), and the SYNC signal (pin 8 of U3).

The basic STATUS signal is produced by wire-AND connecting pins 8 and 10 of U13 (7417) and pin 8 of U14 (7417). The resulting signal passes through a series of open-collector, inverting and noninverting buffers (U21 and U13) after which it is wire-AND connected with the buffered $\bar{S}$ signal. ($\bar{S}$ inhibits the STATUS signal during normal sustain display cycles.) It is then connected to the inputs of four open-collector inverter/buffers (U21 pins 3,9,11, and 13), whose outputs are connected in parallel to increase the status signal's drive capability. The final STATUS output is connected through a 100 ohm resistor to V_{CC} (+5VDC) and then to pin 4 of the interface signal connector (P100). (See section 5.15 for STATUS waveform timing.)

4.1.8 Resistor Pulser (RP) Strobe Generation

The RP Strobe is a LO going pulse which turns on the selected X and Y resistor pulsers at the appropriate time during write and erase operations. It determines the duration and timing of the resulting address pulse. The RP Strobe is derived from the outputs of pin 1 of ROMs U18, U34, and U19; the $\bar{W}$ and $\bar{E}$ signals from the display operation decoder (U5 pins 5 and 6); and the 50KHz output from the ROM address counters (U11 pin 14).

The signals from pin 1 of ROMs U18, U34, and U19 are wire-NOR connected. The resulting signal consists of varying combinations of LO going pulses. The combination present depends upon which of the three ROMs has been enabled. During normal sustain and write cycles, a single pulse occurs during the latter half of the cycle (corresponding to the write address pulse). During erase cycles, two pulses are present; one during each half of the cycle (the first pulse corresponds to the erase address pulse; the second is not used to generate the RP Strobe and is inhibited by the circuit). Two pulses are present during the bulk cycle, but neither is used to generate the RP Strobe and are, therefore, inhibited by the circuit.

The signal from pin 1 of ROMs U19, U34, and U19 is inverted and connected to pins 2 and 11 of U1 (7412).

The $\bar{W}$ and $\bar{E}$ signals from U5 are inverted and connected to pins 9 and 13, respectively, of U1. $\bar{W}$ enables one of the U1 gates during a write cycle and E enables the other during an erase cycle.

The 50KHz squarewave signal is inverted and connected to pin 1 of U1. This signal is HI during the first half of the

display cycles so that, during an erase cycle when pin 13 of U1 is also HI, just the first pulse of the ROM output signal will appear as a LO going pulse at pin 12 of U1.

The 50KHz signal from pin 2 of U2 is reinverted and connected to pin 10 of U1. In this case the signal is HI during the last half of the display cycle so that during a write cycle when pin 9 of U1 is HI, only the last pulse of the ROM output signal will appear as a LO signal at pin 8 of U1.

Pins 8 and 12 of U1 are wire-NOR connected. The resulting RP Strobe signal is buffered by four noninverting buffers for increased drive capability. (See section 5.15 for RP Strobe waveform timing.)

4.1.9 Diode Switch (DS) Strobe Generation

The DS Strobes are LO going signals which turn on the diode switch matrix drive transistors at the appropriate times during all display operations. They are derived from the RP Strobe and the output signal from pin 3 of ROMs U18, U34, and U19.

Pin 3 of ROMs U18, U34, and U19 are wire-NOR connected. The resulting signal consists of varying combinations of LO going pulses. The combination present depends upon which of the three ROMs is enabled.

The signal resulting from the wire-NOR connected ROM outputs is connected to pin 3 of an open-collector buffer, U28 (7417). The RP Strobe from pin 12 of U1 is also connected to an open-collector buffer, U28 pin 1. Pins 4 and 2 of U28 are wire-NOR connected to produce the DS Strobe signal. This signal is connected to the inputs of four open-collector buffers (pins 5,9,11, and 13 of U28) where it is split into four identical signals (DS800T, DS900, DS800B, DS1000).

4.1.10 $\overline{\text{KEYER}}$ Strobe Generation

The $\overline{\text{KEYER}}$ Strobe is a LO going signal used to turn on the X and Y Keyer circuits during write and erase display operations. It is derived from the RP Strobe and the output of ROMs U18, U34, and U19 pin 2.

Pin 2 of ROMs U18, U34, and U19 are wire-NOR connected. The resulting signal consists of varying combinations of LO going pulses. The combination present depends upon which of the three ROMs is enabled. (Not all of the pulses present at the ROM outputs are used to produce the KEYER Strobe signal.)

The signal resulting from the wire-NOR connected ROM outputs is inverted and connected to pin 5 of U3 (7400). A signal from the RP Strobe circuit is connected to pin 4 of U3, and used as a gating signal. The pulse from the ROMs that is coincident with the RP Strobe appears as a LO going pulse at pin 6 of U3. The resulting signal passes through parallel open-collector buffers (U9 - 7417) for increased drive capability. (See section 5.15 for KEYER waveform timing.)

4.1.11 $\overline{XM}$ and $\overline{YM}$ Signal Generation

Pin 3 of ROMs U18, U34, and U19 are wire-NOR connected. The resulting signal consists of varying combinations of LO going pulses. The combination present depends upon which of the three ROMs is enabled.

The signal resulting from the wire-NOR connected ROM outputs is inverted and connected to pins 13 and 2 of U3 (7400). The 50KHz squarewave is inverted and connected to pin 12 of U3, and reinverted and connected to pin 1 of U3. The 50KHz squarewave allows LO going pulses to appear at pins 11 and 3 of U3 during alternate halves of each display cycle.

The signals from pins 3 and 11 of U3 pass through separate open-collector buffers for increased drive capability. (See section 5.15 for XM and YM waveform timing.)

4.1.12 Automatic Bulk Erase

A single bulk erase cycle is automatically initiated after the display has been left idle (normal sustain) for approximately 30 minutes. Automatic bulk erase operations will continue to be initiated at 30 minute intervals for as long as the idle condition persists.

The thirty minute idle period is established by a timer consisting of an oscillator, U15 (NE555); and a 4-bit binary counter, U8 (7493). The output period of U15 is determined by the RC time constant of C18, R8, and R9 (approximately 2 minutes). The

LO going pulses from pin 3 of U15 are counted by U8.

Each time a write, erase, or bulk erase operation occurs, the $\bar{S}$ signal (pin 7 of U5) goes HI. This signal is connected to the reset of U8 (pin 2) so that the counter is reset each time one of these operations takes place. Only when the display is left idle ($\bar{S}$ is LO for at least 30 minutes) will the counter be allowed to reach full count capacity.

When U8 reaches full count capacity, all four of its outputs are HI. This condition is sensed by a circuit consisting of parts of U7 (7412) and U14 (7417). Pins 8 and 12 of U7, which are wire-NOR connected to the C_0 and C_1 control signals, go LO and override the Hi signals present at pins 2 and 4 of U14 (as they are when the display is idle). These LO signals cause a bulk erase operation to be initiated during the next display cycle.

As soon as the bulk erase request is entered into the display operation decoder (U5), the $\bar{S}$ signal goes HI. This resets the counter U8; causing pins 8 and 12 of U7 to float HI.

4.2 200 Board

The 200 board contains the X and Y Resistor Pulser and Keyer circuits. Since the operation of the X and Y circuits are identical, the following explanation of the X resistor pulser and keyer circuits will apply to both (Refer to drawing DD340E0200.)

4.2.1 X Axis Resistor Pulser Circuit

The X resistor pulser circuit consists of 16 resistor pulsers, and the strobe and decoder circuits required to operate them.

X address signals from the 100 board ($\overline{BX1}$, $\overline{BX2}$, $\overline{BX3}$, $\overline{XRB}$ (L), and $\overline{XRB}$ (H)) are connected to the inputs of four BCD-decimal, open-collector decoders (U5, U6, U7, and U8 - 7445). By using only the first 8 outputs from each decoder, it is possible to use pin 12 of each as an enable input. (With pin 12 HI only the unused outputs at pins 8 and 9 will be enabled or, depending upon the input signal combination, all outputs will be floating in the logic "1" state.) The decoder

outputs are connected in parallel as shown for increased current sinking capability.

The decoder enable signals, $\overline{XRP}$ (L) and (H), are normally HI with a LO going pulse of duration and timing appropriate for either a write or an erase address pulse. The occurrence of the LO going pulse on one of the enable signals causes one of the 16 decoder outputs to go LO (the remaining 15 continue to float).

The LO going $\overline{RP\ Strobe}$ signal, produced in coincidence with the decoder enable signal, turns on the strobe transistor, Q38. This completes a current path from signal ground to V_{CC} through the primary of the resistor pulser transformer connected to the LO decoder output. (Transformers isolate the low level inputs from the high level, floating outputs of the resistor pulsers.) The resulting current pulse in the transformer secondary turns on the resistor pulser output transistor. An address pulse is produced with an amplitude essentially equal to the potential of the X pulser supply voltage (V_{AX}).

4.2.2 X Keyer Circuit

The LO going $\overline{KEYER}$ signal turns on Q39 which in turn turns on Q40. This allows current to flow through the primary of the keyer circuit isolation transformer. The resulting current pulse in the transformer secondary turns on the keyer output transistor Q34, producing a pulse with an amplitude essentially equal to the potential of the X pulser voltage supply (V_{AX}).

4.3 300 Board

The 300 board contains the sustainer circuits for the X and Y axes, and the voltage regulator for V_{MX} and V_{MY}. (Refer to drawing DD340E2100.)

4.3.1 X and Y Sustainer Circuits

The X and Y sustainer circuits are essentially identical with each consisting of a "pull-up" circuit (XUS, YUS) which pulls the respective sustainer waveform to V_{SS}; a "pull-medium" circuit (XM, YM) which pulls the waveform to V_{MX} or V_{MY} as

appropriate; and a "pull-down" circuit (XDS, YDS) which pulls the waveform to sustainer ground (signal ground). The XUS, YUS, XDS, and YDS circuits are similar and the following explanation of the XDS circuit will apply to each.

The LO going turn-on signal from the 100 board, $\overline{XD}$, passes through two transistors connected in a darlington configuration (Q30, Q31) to turn on Q17. This discharges capacitor C11 through the primary of the isolation transformer, T11. A 5 ampere current pulse, induced in the T11 secondary, is supplied to the base of the output transistor, Q8; turning it on. This turn-on pulse must keep Q8 in saturation for approximately 4.5 nanoseconds to maintain the integrity of the output signal (sustainer waveform voltage level).

A separate turn-off signal is used to insure that the output transistor, Q8, is off when either of the other X sustainer circuits is turned on. This signal, $\overline{XD}$°, turns on Q29 and in turn Q16, allowing current to flow through the primary of the isolation transformer, T10. The resulting current in the secondary is forced into the base of Q8, turning Q8 off quickly. (Q8 must turn off within 1200 nanoseconds after the turn-off signal is applied.)

The XM and YM circuits are similar and the following explanation of the XM circuit will apply to each.

The LO going $\overline{XM}$ signal from the 100 board turns on Q24, allowing current to flow through the isolation transformer, T6. The resulting current pulse in the secondary turns on the output transistor, Q4. A resistor, R10, connects the base of Q4 to sustainer ground (signal ground). R10 aids in turning Q4 off by providing a path for current into the base circuit after the turn on signal has been removed.

4.3.2 V_{MX} and V_{MY} Regulator

The V_{MX} and V_{MY} voltages are derived from the V_{SS} supply by a single regulator circuit. This circuit consists of a simple darlington amplifier. The output voltage, which is adjustable through R73, is supplied to both the XM and YM circuits.

4.4 400, 500, 600, and 700 Boards

The 400, 500, 600, and 700 boards contain the diodes and resistors for the diode/resistor matrix associated with each of the four sides of the display panel. Refer to drawings DD340E400 through 700 for interconnections on these boards. (See sections 2.0 and 3.0 for an explanation of the diode/resistor matrix.)

4.5 800 Board

The 800 board contains one X axis diode switch matrix circuit. (Two 800 boards are used in the display system: One associated with the even X electrodes, the other with the odd X electrodes. The two boards are designated 800B and 800T respectively.) The following explanation of this board should be accompanied by drawing DD340E0800.

The diode switch matrix circuit consists of a 4 x 4 diode matrix along with the required drive transistors, decoder, and strobe circuits.

X address bits and enable signals from the 100 board ($\overline{BX5}$, $\overline{BX6}$, $\overline{BX7}$, $\overline{BX8}$, $\overline{Xeven}$, and $\overline{Xodd}$) are connected to the inputs of two BCD-decimal, open-collector decoders (U1 and U2 - 74145). Since only the first four outputs of each decoder is used, pin 12 of each can be used as an enable input, (all decoder outputs float until enabled, at which time one in each decoder goes LO).

At the appropriate times during every display cycle, the DS Strobe signal (DS800T or DS800B) is used to turn on transistor Q1, and in turn the DS strobe transistor, Q2. This completes a current path from signal ground to V_{CC} through the primary of all 8 isolation transformers connected to the matrix drive transistors. (Transformers isolate the low level inputs from the high level, floating outputs of the matrix drive transistors.) The resulting current pulse in the transformer secondaries turns on all 8 matrix drive transistors. (A complete current path then exists between the XDS and XUS sustainer circuits and each of the 16 diode matrix outputs.)

At the same time that an address pulse is produced by the resistor pulser (during a write or erase operation), the DS strobe transistor is turned on and the matrix transistor decoders (U1 and U2) are enabled. One of the outputs in each decoder goes LO.

This shunts the current from the two transformer primaries connected to the LO outputs, preventing one drive transistor on each side of the diode matrix from being turned on. (The current path between the matrix output common to these two transistors, and the X sustainer circuits is broken.)

4.6 900 Board

The 900 board contains the diode switch matrix circuit associated with the odd Y electrodes. The operation of the Y diode switch matrix circuit is similar to that of the X circuit on the 800 board. (Refer to drawing DD34E0900.)

4.7 1000 Board

The 1000 board contains the diode switch matrix circuit associated with the even Y electrodes; and the X and Y border sustainer circuits. (Refer to drawing DD34E1000.)

4.7.1 Y Diode Switch Matrix Circuit

The operation of the Y diode switch matrix circuit is similar to that of the X circuit on the 800 board.

4.7.2 X and Y Border Sustainer Circuits

The X and Y BORDER SUSTAINER circuits are identical with both consisting of a "pull-up" (XUB, YUB) and "pull-down" (XDB, YDB) circuit. The following explanation of the X border sustainer circuit will also apply to the Y circuit.

The XDB circuit pulls the X border sustainer output to the sustainer ground level (signal ground) in response to a LO going pulse, $\overline{\text{XDB}}$, from the 100 board. This pulse turns on Q19 and in turn, Q20. A HI signal appears at the base of the "pull-down" output transistor, Q21, turning it on so that its collector and the X border sustainer go to ground. (Since the base of the "pull-up" transistor, Q22, is connected to the collector of Q21, it is insured that Q22 is turned off.)

When the collector of Q21 goes LO, current flows through the primary of transformer T6. This causes a negative feedback signal to be applied to the base of Q21, preventing it from going into saturation and allowing it to turn off quickly when required to do so. In addition, the negative feedback circuit tends to turn off Q21 should it begin to conduct without a turn-on signal being present.

The XUB circuit pulls the X border sustainer output to the border voltage level ($V_{SS}+V_{SB}$) in response to a LO going pulse, XUB, from the 100 board. This pulse turns on Q17 and in turn Q18, allowing current to flow through the primary of the isolation transformer. The resulting positive going pulse appears at the base of the output transistor, Q22. (The base-emitter circuit of Q22 is at ground during this time.) Q22 turns on, pulling its base-emitter circuit and the border sustainer output to the border voltage level.

5.0 MAINTENANCE

5.1 Troubleshooting Chart

Starts on next page

In most cases a defective circuit or out-of-adjustment voltage level will first be recognized as improperly displayed information in the display panel. Through careful comparison of the defectively displayed information with the symptoms listed in the troubleshooting chart (which starts on page 35) BEFORE the actual repair work is started, much time can be saved in locating the fault. It may be helpful to make a sketch or take a picture of the defectively displayed information to use as a reference while repairs are made.

The symptoms listed in the troubleshooting chart assume that only one fault is involved and in only one axis. Multiple faults may result in unusual combinations of symptoms which may be difficult to separate. The possible causes that are listed refer in most cases to the circuits associated with just the affected electrode(s).

5.2 Printed Circuit Extender Boards

Printed circuit card extenders for the following boards are available through our service department:

Board*	Part Number
100	CD340C1700
200	CD340C1900
300	CD340C1600
800 and 900	CD340C1800
1000	CD340C1500

*400, 500, 600, and 700 boards do not require extenders for troubleshooting.

5.3 Display Troubleshooting Using S159/205 Power Pack Voltages

When the S159/205 power pack is used to power the display during troubleshooting, voltages that are not required for a given checkout procedure must be disabled. This is done by removing the fuse associated with each of these voltages. (See UM609 for S159/205 power pack fuse locations.)

5.4 Printed Circuit Board Locations

Figure 5.1 illustrates the locations of the printed circuit boards used in the display. The display unit is shown from the rear, with its rear cover removed and in an upright position. (Note that the printed circuit boards plug into a motherboard which is not shown in the figure.)

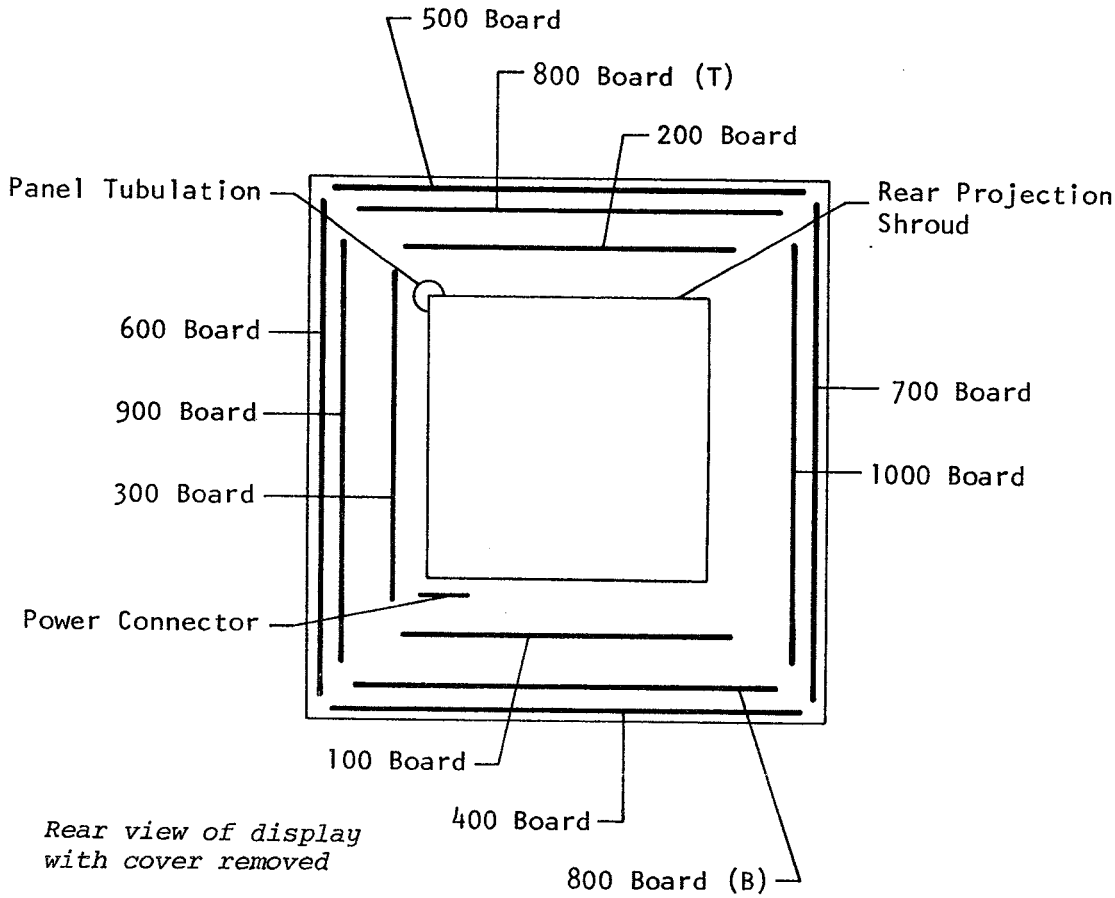


Figure 5.1 - Printed Circuit Board Locations

SYMPTOM	POSSIBLE CAUSE	ACTION	POWER SUPPLY REQUIRED
A) Blank panel - no borders*	Faulty AC power source	Verify power to display	None
	Loose power interconnect cable Missing or low V_{CC} Missing or low V_{SS} Missing or low V_{SB} No V_{SB} boost level	Remove AC Power FIRST, then disconnect power input connector and verify each power supply voltage (See UM607 for power connector pin assignments) (See Note 1)	None
	Faulty control/interface logic (100 board)	Verify timing of sustainer and border sustainer logic signals from 100 board	V_{CC} only
	Faulty sustainer or border sustainer circuits	See sustainer and border sustainer troubleshooting section 5.12	
	Broken panel	Check panel and tubulation for breakage	
	*Occasionally after the display has not been used for an extended period of time, the borders may not "light" when AC power is first applied.	Remove AC power and wait approximately 10 seconds before reapplying in order to "light" the borders (Repeat as required)	None

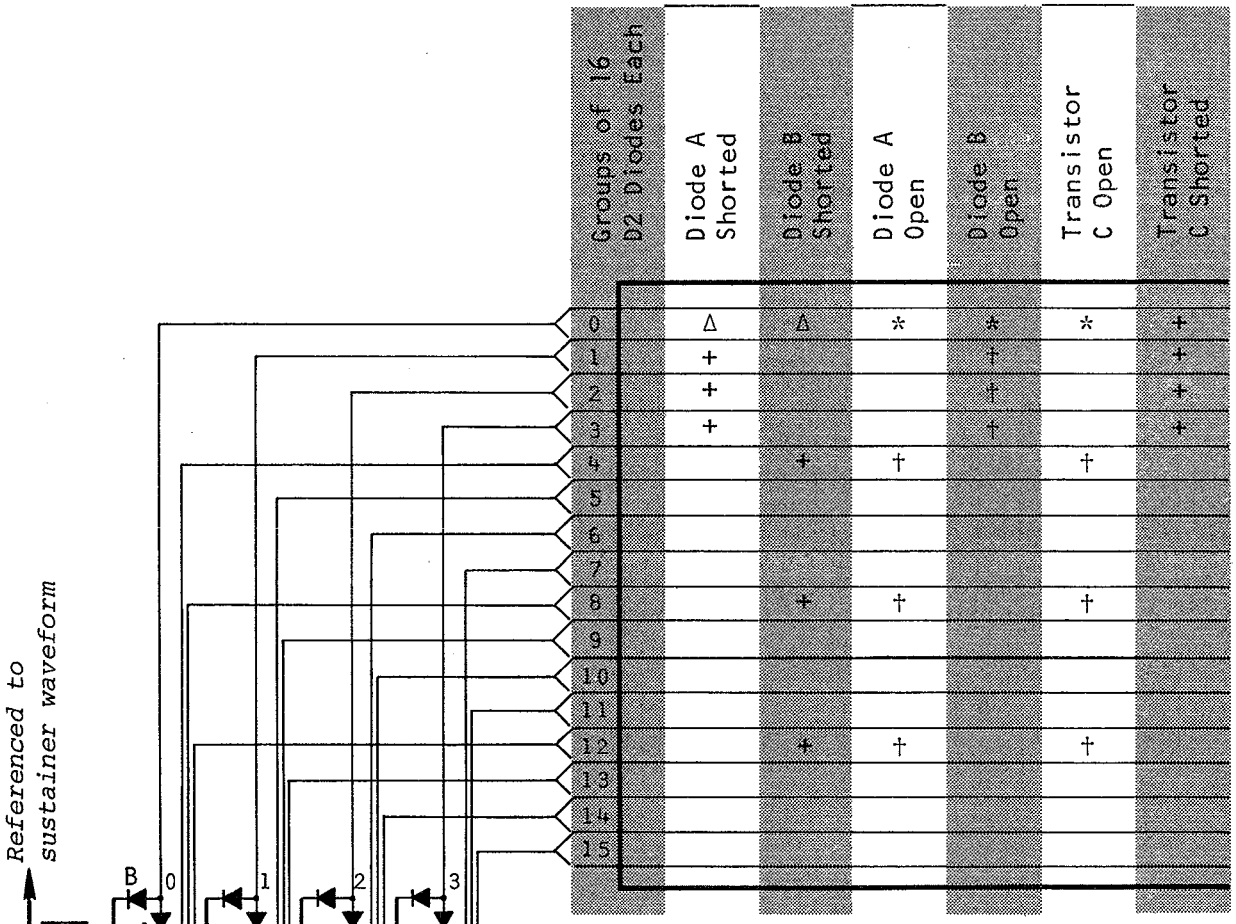
1. If the S159 power pack is used to power the display, refer to MM610 for procedures for troubleshooting missing or low voltages.

SYMPTOM	POSSIBLE CAUSE	ACTION	POWER SUPPLY REQUIRED
B) Panel Blank - with borders	Faulty interface signal connection or timing	Verify proper signals at interface connector (See UM607 for interface signal timing and connection)	None
	Faulty control/interface logic (100 board)	Verify control signal input and display operation selection logic; SYNC, STATUS, RP Strobe, DS, and Keyer signals; and check for possible continuous automatic bulk erase request	V_{CC} only
	Missing or Low V_{AX} or V_{AY}	Verify V_{AX} and V_{AY} at 200 board	V_{CC}, V_{AX}, V_{AY}
	Missing or improperly adjusted sustainer waveform medium levels	Check X and Y sustainer waveforms for V_{MX} and V_{MY} levels (V_{MX} and V_{MY} = approx. 36VDC, see section 5.13 for adjustment procedure)	All
		If V_{MX} or V_{MY} is missing:	
		1) Check $\overline{XM}$ and $\overline{YM}$ logic signals on 100 board	V_{CC} only
		2) Check V_{MX}/V_{MY} regulator on 300 board	All
		3) Check XM and YM sustainer circuits (see section 5.11 for sustainer troubleshooting)	

C) One or more borders missing	Open circuit between border sustainer and electrodes	Check continuity of border output conductors	None
	Low border voltage ($V_{SS}+V_{SB}$)	Verify proper V_{SS} + V_{SB} level at border sustainer circuits (1000 board)	V_{CC}, V_{SC}, V_{SS}, V_{SB}
	Faulty border sustainer circuit	See section 5.12 for border sustainer troubleshooting	
D) Borders remain bright after turn-on	V_{SB} does not drop back to normal operating level after boost period	Check power supply setup (See Note 1, page 37)	None
E) Eratic write and/or erase over entire or large parts of panel	Improper system grounding* (signal and chassis grounds)	Remove AC power and check continuity of signal and chassis grounds. *Try using a different way of connecting signal and chassis grounds together (i.e. decoupling capacitors versus direct connection; different connection point).	None
	Improper interface signal timing	Refer to UM607 for proper interface signal timing	None
	Improper voltage adjustment (V_{SS}, V_{AX}, V_{AY} or V_{CC})	Verify proper voltage levels at each circuit board (see UM607 for voltage readjustment procedure)	All
	Continued		

SYMPTOM	POSSIBLE CAUSE	ACTION	POWER SUPPLY REQUIRED
E) Continued	Missing or improperly adjusted sustainer waveform medium levels	1) Check $\overline{XM}$ and $\overline{YM}$ logic signals on 100 board 2) Check V_{MX}/V_{MY} regulator on 300 board 3) Check XM and YM sustainer circuits (see section 5.12 for sustainer troubleshooting)	V_{CC} only All
	Defective $\overline{\text{RP Strobe}}$, DS, or $\overline{\text{Keyer}}$ signal	Verify appropriate signal amplitude and waveform at 100, 200, 800(T), 800(B), 900 and 1000 boards	V_{CC} only
F) Writes properly, but points go out as display capacity is approached	Current limiting circuit in S158	See Note 1, page 37	
	Low V_{SS}	See UM607 for voltage readjustment procedure	
G) Writes properly, but does not erase or does so poorly	Improperly adjusted voltage levels	See UM607 for voltage readjustment procedure	
	Faulty erase logic on 100 board	Check for $\overline{\text{RP Strobe}}$, DS, and $\overline{\text{Keyer}}$ signals during erase cycle	V_{CC} only
	Y sustainer medium level missing	1) Check $\overline{XM}$ and $\overline{YM}$ logic signals on 100 board 2) Check V_{MX}/V_{MY} regulator on 300 board 3) Check XM and YM sustainer circuits (see section 5.12 for sustainer troubleshooting)	V_{CC} only All

H) Erases properly, but does not write or does so poorly	Improperly adjusted voltage levels	See UM607 for voltage readjustment procedure	
	Faulty write logic on 100 board.	Check for $\overline{\text{RP Strobe}}$, DS, and $\overline{\text{Keyer}}$ signals during write cycle	V_{CC} only
	X sustainer medium level missing	1) Check $\overline{XM}$ and $\overline{YM}$ logic signals on 100 board	V_{CC} only
		2) Check V_{MX}/V_{MY} regulator on 300 board	All
		3) Check XM and YM sustainer circuits (see section 5.11 for sustainer troubleshooting)	
I) 16 (or multiples of 16) alternate electrodes cannot be addressed	Faulty diode switch matrix circuit	See chart in figure 5.2 (Check suspected components with an ohmmeter)	None
	Open circuit between diode switch matrix output and diode/resistor matrix	Check continuity of conductors	None
	Faulty diode switch matrix decoder output (output always floats)	Check decoder outputs during operation	V_{CC} only
J) 16 alternate electrodes are addressed when they are not supposed to be	Faulty diode switch matrix circuit	See chart in figure 5.2 (Check suspected components with an ohmmeter)	None
	Faulty diode switch matrix decoder output (output always LO)	Check decoder outputs during operation	V_{CC} only



Diode Switch Matrix Circuit

(associated with even or odd X electrodes)

Diode A or B Shorted - Groups marked + will not work when selected; Δ and all others appear OK.

Diode A or B Open - All groups appear to work OK when selected; however, * will also be selected in coincidence with each † group.

Transistor C Open - All groups appear to work OK when selected; however, * will also be selected in coincidence with each † group as shown above. (Similarly: 1 coincident with 5,9, & 13; 2 with 6,10, & 14; and 3 with 7, 11, & 15.)

Transistor C Shorted - Groups marked + will not work when selected; all others OK.

Figure 5.2 - Diode Switch Matrix Troubleshooting Chart

SYMPTOM	POSSIBLE CAUSE	ACTION	POWER SUPPLY REQUIRED
K) 2 adjacent electrodes (repeating every 32) write and erase when not addressed	Resistor pulser transistor shorted	Check suspected faulty components with ohmmeter or Check resistor pulser circuits in dynamic operation	None V_{CC} and V_{AX} or V_{AY}
	Faulty resistor pulser decoder (output always LO)	Check decoder outputs during operation	V_{CC} only
L) 2 adjacent electrodes (repeating every 32) never addressed	Resistor pulser transistor open	Check suspected faulty components with ohmmeter or Check resistor pulser circuits in dynamic operation	None V_{CC} and V_{AX} or V_{AY}
	Open circuit between resistor pulser and diode/resistor matrix	Check continuity of conductors	None
	Faulty resistor pulser decoder (output always floats)	Check decoder outputs during operation	V_{CC} only
M) 2 alternate electrodes do not write or erase or do so erratically	Shorted conductors (connected to affected electrodes) between panel and diode/resistor matrix	Use ohmmeter to locate shorted conductors (Note: Do not attempt to repair shorts on panel - see section 5.9)	None
N) Single electrode cannot be addressed (no border discharges on electrode)	Open circuit between panel and diode/resistor matrix	Check for continuity of conductors with ohmmeter (Note: Do not attempt to repair open conductors on panel - see section 5.9)	None

SYMPTOM	POSSIBLE CAUSE	ACTION	POWER SUPPLY REQUIRED
O) Single electrode cannot be addressed (border discharges present on electrode)	Open diode or resistor, or shorted D1 diode in diode/ resistor matrix	Check suspected faulty components with ohmmeter	None
P) Single electrode writes and erases when not addressed	Shorted D2 diode in diode/resistor matrix	Check suspected faulty components with ohmmeter	None
Q) All odd or even electrodes in a given axis cannot be addressed (No border discharges present on affected electrodes)	Open conductor between sustainer circuit and diode/resistor matrix	Check continuity of conductors	None
R) All odd or even electrodes in a given axis cannot be addressed (borders ok)	Missing DS Strobe signal or faulty strobe circuit in diode switch matrix circuit	Check for presence of DS signal Check diode switch strobe circuit	V_{CC} only V_{CC} only
S) Groups of adjacent electrodes repeating across entire display panel cannot be addressed (borders ok)	Groups composed of every other: electrode - address bit 0 faulty 2 electrodes - " " 1 " 4 electrodes - " " 2 " 8 electrodes - " " 3 " 16 electrodes - " " 4 " 32 electrodes - " " 5 " 64 electrodes - " " 6 " 128 electrodes - " " 7 " 256 electrodes - " " 8 "	Check interface signals and interface logic on 100 board	V_{CC} only
T) Orange glow over entire display panel	Missing sustainer medium levels	Check for faulty $\overline{XM}$ and $\overline{YM}$ signals on 100 board Check for faulty drive transistors in XM and YM sustainer circuits (see section 5.12)	V_{CC} only

5.5 Alternate 400, 500, 600, and 700 Boards

Either of two types of 400, 500, 600, or 700 board may be used in this display. One type is assembled using all discrete components. The other type uses discrete resistors, but all diodes are in dual-in-line packs. Corresponding boards of each type are completely interchangeable.

The following chart describes the interchangeability between these various boards:

X Even Matrix (400 board)
CD340D0400 (discrete) ← → CD340D2400 (dual-in-line)

X Odd Matrix (500 board)
CD340D0500 (discrete) ← → CD340D2400 (dual-in-line)

Y Odd Matrix (600 board)
CD340D0600 (discrete) ← → CD340D2600 (dual-in-line)

Y Even Matrix (700 board)
CD340D0700 (discrete) ← → CD340D2700 (dual-in-line)

5.6 Rear Cover Removal

WARNING

Hazardous voltages are present inside the display. Disconnect AC power before removing the cover.

To remove the rear cover from the display and gain access to the printed circuit boards:

1) Disconnect the system from the AC power source.

2) Disconnect the power and interface signal cables from the display unit.

3) Place the display unit face down on a clean, soft surface.

4) Remove the eight Phillips head screws from the sides, top, and bottom of the rear cover (do not remove the eight similar screws from the front cover).

5) Carefully lift the rear cover straight up and off.

5.7 Electronic Component Outline Drawings

Most electronic components used in the display system have standard electronic and mechanical configurations. Outline drawings for the few special electronic components used in the display are illustrated in figure 5.3.

5.8 How to Observe the Composite Sustainer Waveforms

The composite sustainer waveforms may be observed as they are illustrated in this manual by using a differential oscilloscope (or one with dual vertical amplifiers, and the capability to add the amplifier outputs). Connect the X sustainer waveform to the noninverting input (+) of the oscilloscope, and the Y waveform to the inverting input (-). (A typical composite sustainer waveform is illustrated on page 51.)

5.9 Display Panel and Ribbon Cable Defects

WARNING

DO NOT ATTEMPT TO REPAIR the display panel or the bonds between it and the ribbon cables.

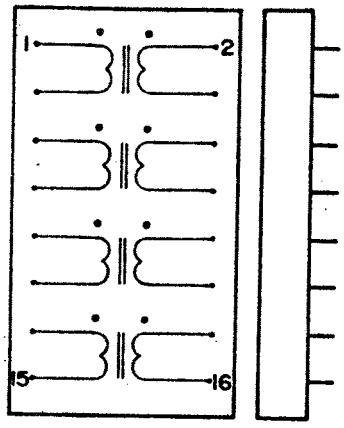
Contact our service department at (419) 242-6543, ext. 66-217 for instructions regarding a defective display panel and/or ribbon cable.

5.10 Display Panel Ribbon Cable Removal and Reassembly

CAUTION

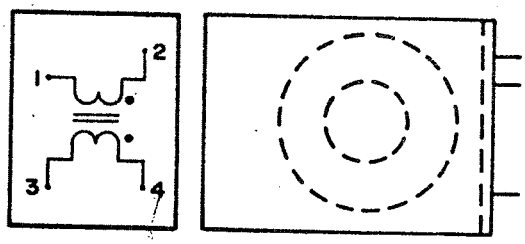
Do not remove the panel ribbon cables from the 400, 500, 600, or 700 board unless necessary. (Most troubleshooting on these boards can be done with the cables attached.)

TRANSFORMER



7220-1005

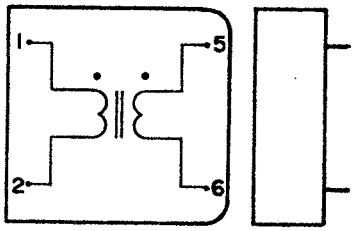
TRANSFORMER



01 300100
01 300200
01 300300

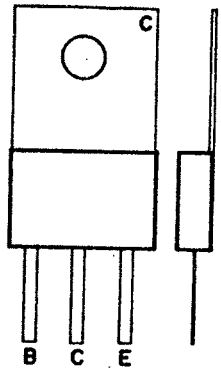
also unpotted

TRANSFORMER



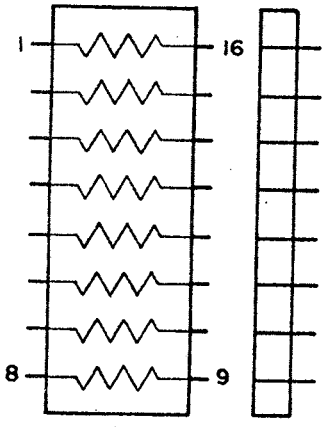
7120-1019

TRANSISTOR



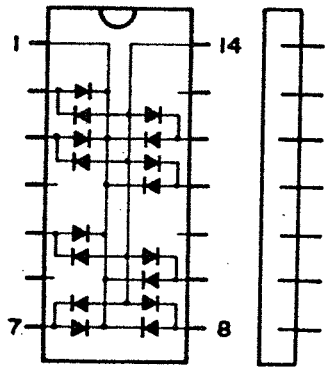
All "TIP" Series
D45H1
D45C3

RESISTOR ARRAY



CTS 15R-1K

DIODE PAC



DA 210

Figure 5.3 - Electronic Component Outline Drawings

WARNING

Do not pull, twist, or otherwise place strain upon the ribbon cables connecting the display panel to the 400, 500, 600, and 700 boards. To do so may permanently destroy or impair the usefullness of the display panel.

Ribbon cables are used to connect the display panel to the 400, 500, 600, and 700 boards. To disconnect the ribbon cables from one of these boards:

1) Loosen the screws on the clamping bar (located along the edge of the board near the motherboard) until the cables can be moved. (If only one cable is to be removed, loosen only the screws immediately beside it.) Be careful not to disturb the alignment of the cables that are not to be removed.

2) Without pulling on the display panel end of the ribbon cable(s), carefully slide the cable(s) out from under the clamping bar.

To reassemble the ribbon cables to the 400, 500, 600, or 700 board:

1) Loosen the clamping bar screws near where the cable will be inserted just enough to allow the cable to be "wiggled" under the clamping bar.

2) Push the ribbon cable until approximately 1/32nd of an inch of the cable projects beyond the opposite side of the clamping bar.

3) Move the ribbon cable until the conductors in the cable are in registration with the conductors on the printed circuit board.

4) Tighten the screws on either side of the cable just enough to prevent it from losing its alignment.

5) After all cables have been reassembled, tighten all clamping bar screws.

6) IMPORTANT - Before attempting to apply any power to any display circuits, check to insure that a short circuit does not exist between any adjacent conductors

in the ribbon cables. This can be done by using an ohmmeter to probe the conductors on the printed circuit board along the edge of the clamping bar. The resistance between adjacent conductors should exceed 100K ohms. Any short circuits found MUST be repaired before power is restored to the display.

5.11 Display Panel Removal and Reassembly

To remove the display panel from the chassis:

1) Remove the rear cover from the display unit (see section 5.6 for procedure).

2) Remove all the display panel ribbon cables from the 400, 500, 600, and 700 boards (see section 5.10 for procedure and warning note).

3) Position the display unit with the display panel facing upward.

4) Remove the eight Phillips head screws from the sides, top, and bottom of the front cover.

5) Remove the four slotted flat head screws from the front surface of the front cover.

6) Carefully lift the front cover straight up and off.

7) Mark the position of the display panel in some manner so that the panel can be replaced in the same position.

8) Using a wooden tongue depressor or similar non-metallic instrument, gently pry the display panel from its silicone rubber mounting pads.

9) Lift the display panel from the chassis, being careful that strain is not placed on the ribbon cables or the display panel tubulation.

To reinstall the display panel reverse the foregoing procedure. Before replacing the screws in the front cover, insure that the display panel active area electrodes are centered in the front cover opening.

5.12 Troubleshooting Sustainer and Border Sustainer Circuits

1) Remove the rear cover from the display (see section 5.6 for procedure).

2) Use extender cards to place the 300 and 1000 boards outside the display for troubleshooting (see section 5.2 for information regarding the availability of extender cards). (To remove the 300 board, it is necessary to remove five slotted head screws which secure the heat sinks to the rear projection shroud.)

3) Reattach the power input connector and apply ONLY V_{CC} and V_{SC} (5VDC and 9VDC respectively).

4) Using an oscilloscope with a clamp-on current probe, compare the waveform of the current flowing through the collector of each sustainer and border sustainer output transistor with the waveforms shown on the following pages. (Current probe should be clamped to the wire connecting each output transistor to the printed circuit. The oscilloscope should be triggered on the SYNC output signal.)

5) The entire circuit associated with an output transistor that has an abnormal current waveform should be checked for faulty components. This can be done by checking the circuit with an ohmmeter for open or shorted components; particularly open or shorted transistors, diodes, and transformers.

6) Replace faulty components and again compare the current waveforms with those shown on the following pages.

7) Verify proper operation of the display using all voltages. (Note: all rise and fall times of the sustainer and border sustainer waveforms must be less than or equal to 300 nanoseconds. A typical waveform is shown on page 54.)

8) Remove AC power and reinstall the 300 and 1000 boards, and the rear cover. (Be sure to secure the heatsinks on the 300 board to the rear projection shroud using the screws removed in step 2.)

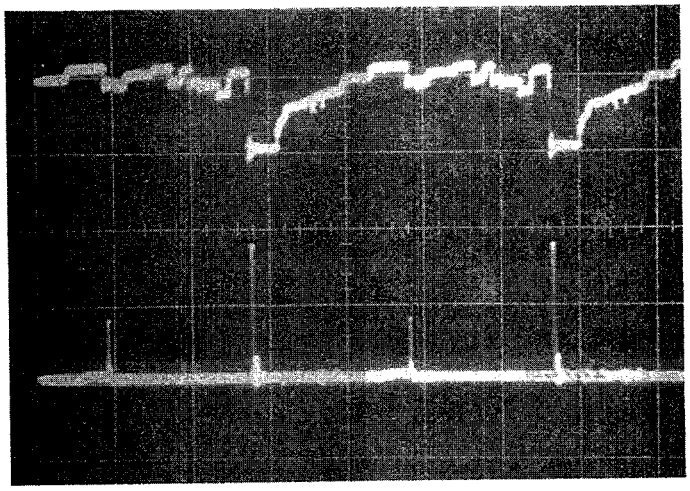
5.13 V_{MX}/V_{MY} Adjustment

The sustainer medium voltages, V_{MX} and V_{MY}, are derived from the sustainer voltage (V_{SS}) by a circuit inside the display (see section 4.3.2 for circuit description). The output voltage level of this circuit, which is common to both V_{MX} and V_{MY}, is preset and should not require readjustment except in the case where the regulator has been repaired. If necessary, the voltage level can be readjusted as follows (continued on page 51):

Horizontal deflection - 5μsec/cm

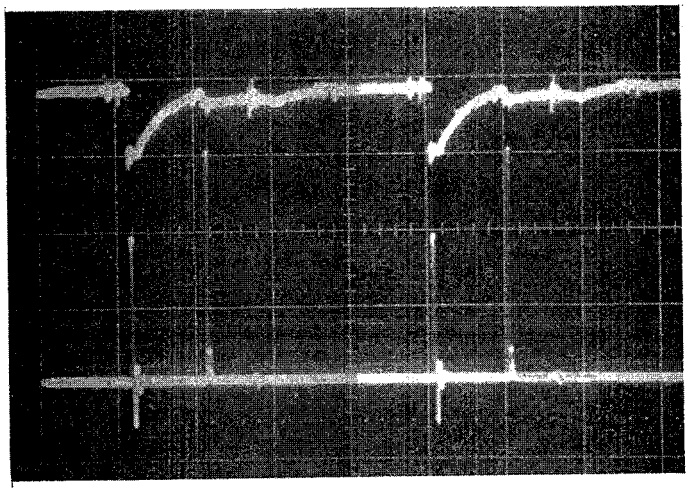
XUS Q19 base
5VDC/cm

Q1 collector
1A/cm



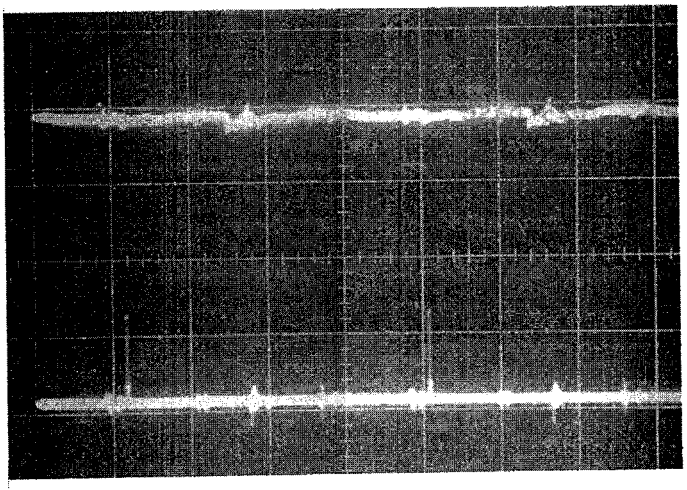
XDS Q30 base
5VDC/cm

Q8 collector
1A/cm



XMS Q24 base
5VDC/cm

Q4 collector
100mA/cm

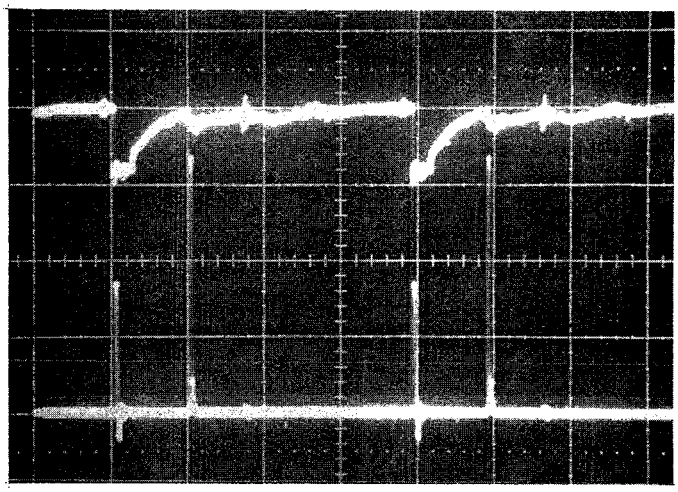


Current waveforms with V_{CC} and V_{SC} ONLY.

Horizontal deflection - 5µsec/cm

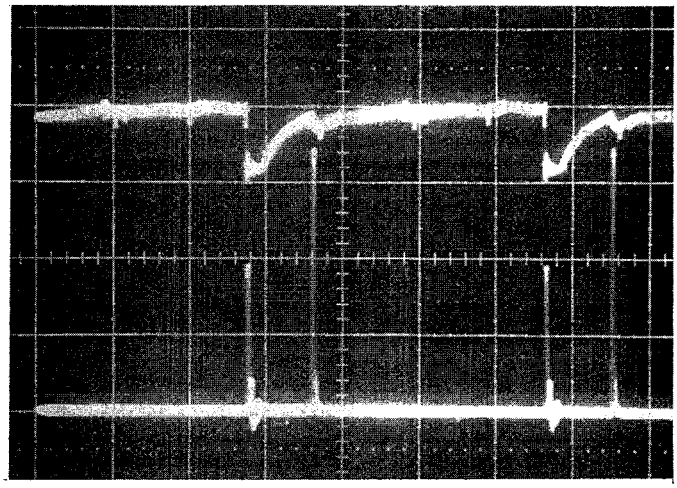
YUS Q27 base
5VDC/cm

Q7 collector
1A/cm



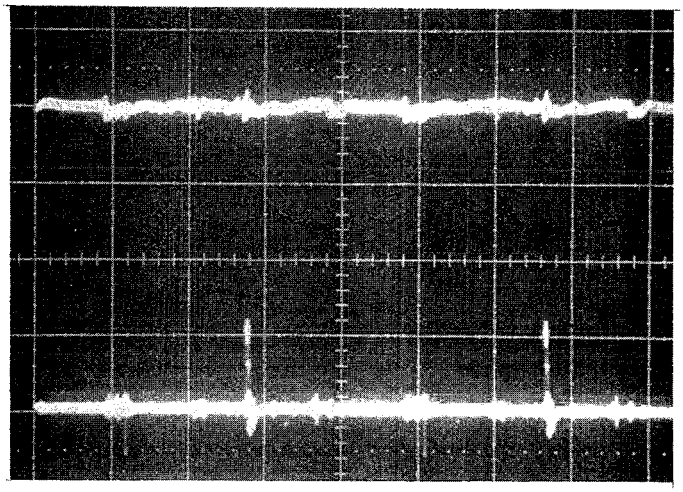
YDS Q22 base
5VDC/cm

Q2 collector
1A/cm



YMS Q25 base
5VDC/cm

Q6 collector
100mA/cm

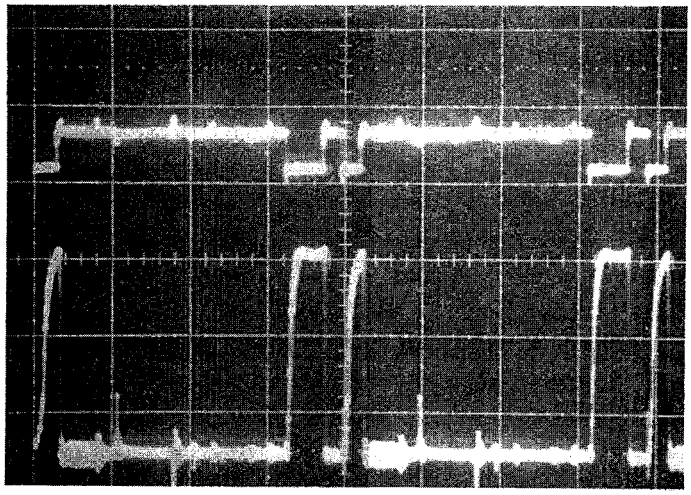


Current waveforms with V_{CC} and V_{SC} ONLY.

Horizontal deflection - 5μsec/cm

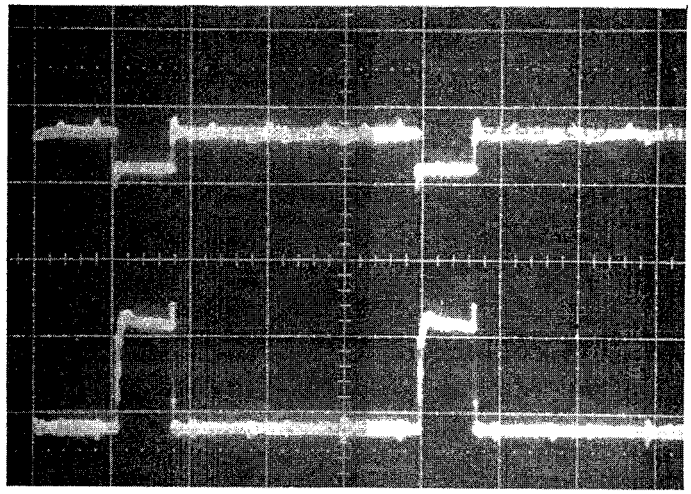
XUB Q17 base
5VDC/cm

Q22 collector
200mA/cm



XDB Q19 base
5VDC/cm

Q21 collector
200mA/cm

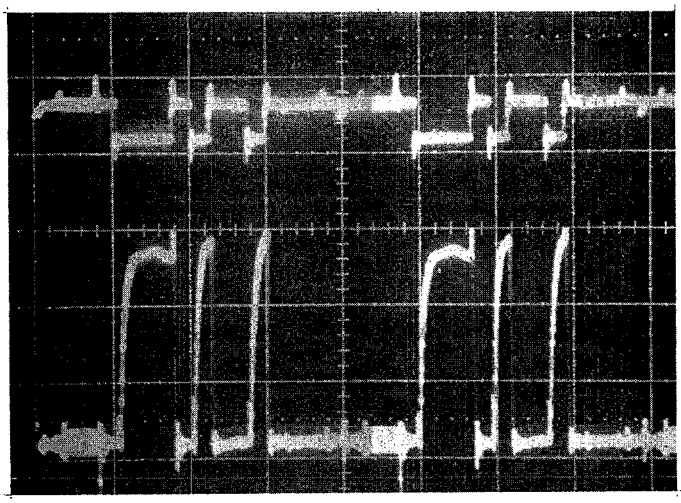


Current waveforms with V_{CC} and V_{SC} ONLY.

Horizontal deflection - 5µsec/cm

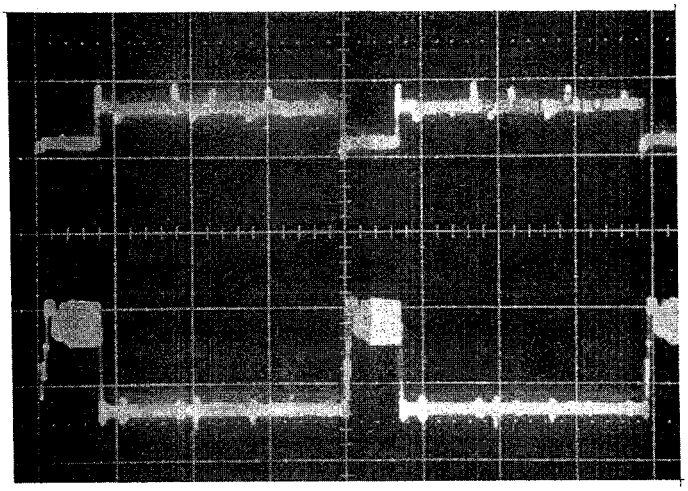
YUB Q11 base
5VDC/cm

Q16 collector
200mA/cm



YDB Q13 base
5VDC/cm

Q15 collector
200mA/cm



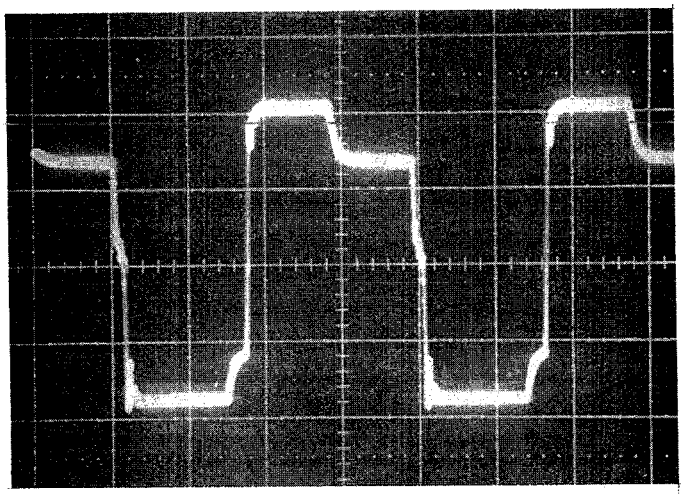
Current waveforms with V_{CC} and V_{SC} ONLY.

TYPICAL COMPOSITE SUSTAINER WAVEFORM

Horizontal-5µsec/cm
Verticle-50VDC/cm

Y

X



1) Remove the rear cover from the display (see section 5.6 for procedure).

2) With AC power OFF, reattach the power input connector.

3) Apply all voltages to the display as when the display is in normal operation.

> CAUTION
>
> Hazardous voltages exist inside the display. Use caution when operating the display with its cover removed.

4) Using a DC voltmeter referenced to signal ground, measure the voltage on the case (collector) of Q5 on the 300 board. This is the V_{MX}/V_{MY} voltage level.

5) Readjust this voltage to 36 VDC by adjusting R73 on the 300 board. (Use a nonconductive screwdriver.)

6) If necessary, go through the voltage readjustment procedures listed in UM607 (or UM609 if the S159 power pack is being used to power the display) to restore proper display operation.

7) Remove AC power and reassemble the display.

5.14 5VDC Output Fuse Replacement

To replace the fuse that protects the 5VDC output (pin 2 of the interface signal connector):

1) Disconnect the system from the AC power source.

2) Using the procedure in section 5.6, remove the rear cover from the display.

3) Locate the black ground wire that runs between the 100 board and the motherboard (see figure 5.1 for board location). Remove the screw that secures the wire to the motherboard.

4) A black plastic bracket is attached to the 100 board. Remove the screw and washer securing this bracket to the motherboard.

5) Carefully unplug the 100 board assembly from the motherboard and remove it from the display.

6) Locate F1 on the 100 board (see assembly drawing DD340C2000) and test the fuse for continuity. Replace it if necessary.

To reinstall the 100 board, reverse the foregoing procedure.

5.15 Logic Signal and ROM Timing Charts

Start on next page

5.16 Ordering Replacement Parts

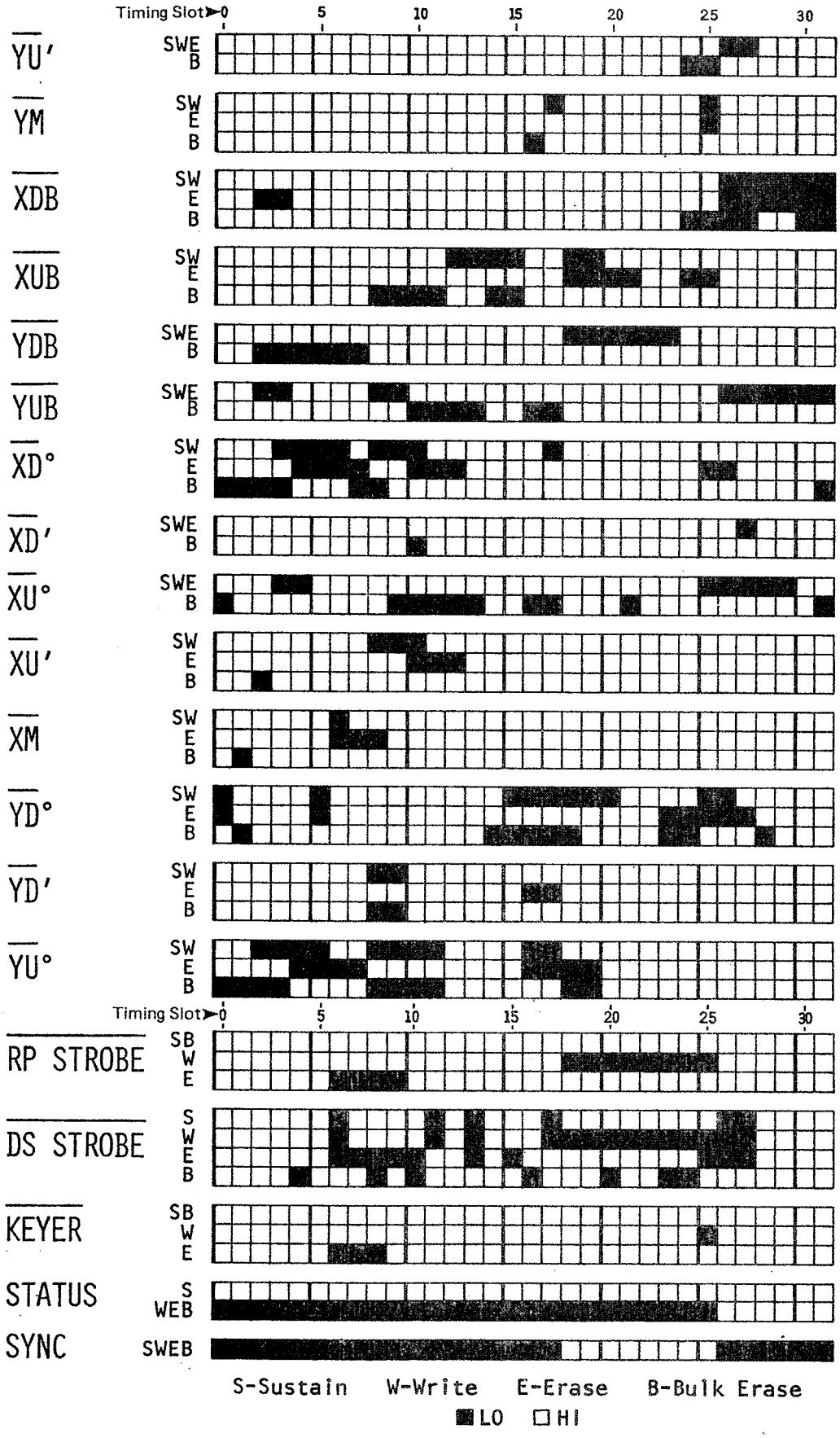
When ordering replacement parts, include the product and serial numbers of the display, a brief description of the part, its part number, and the number of pieces required. Orders should be sent to:

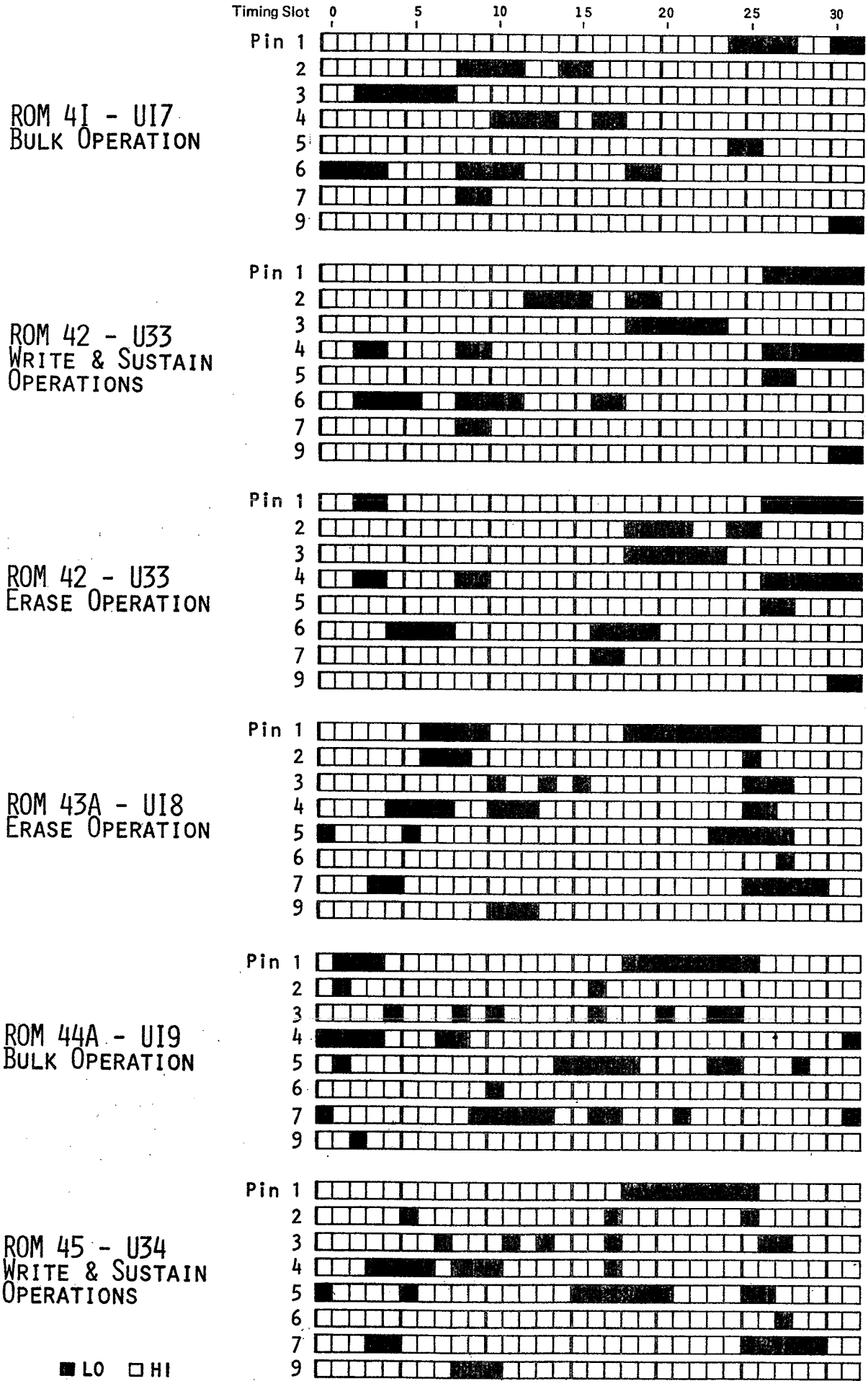
Owens-Illinois, Inc.
Electro/Optical Display Operation
ATTN: Field Service Manager
PO Box 1035
Toledo, Ohio 43666

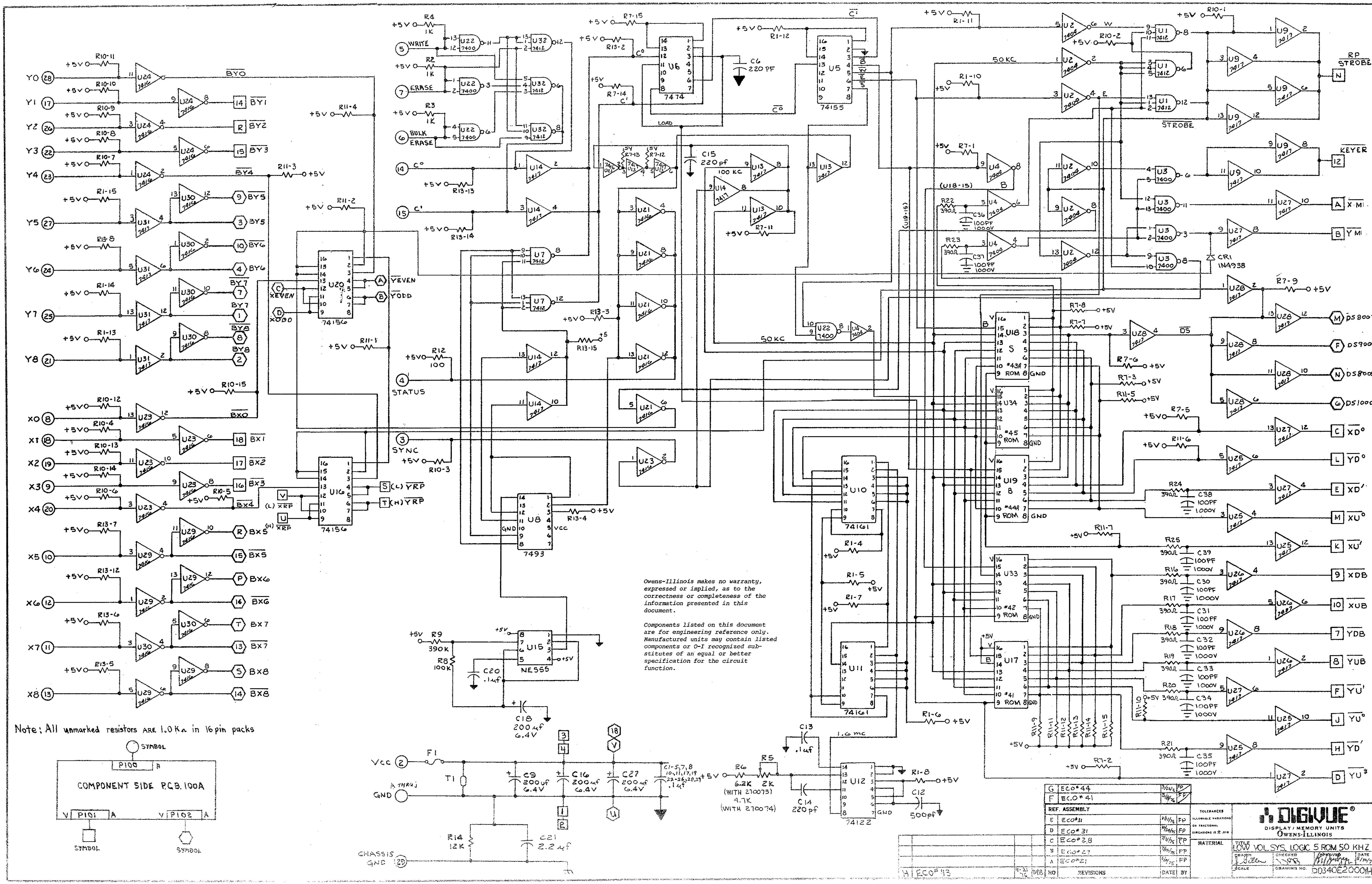
5.17 Electronic and Mechanical Drawings

Start on page 59

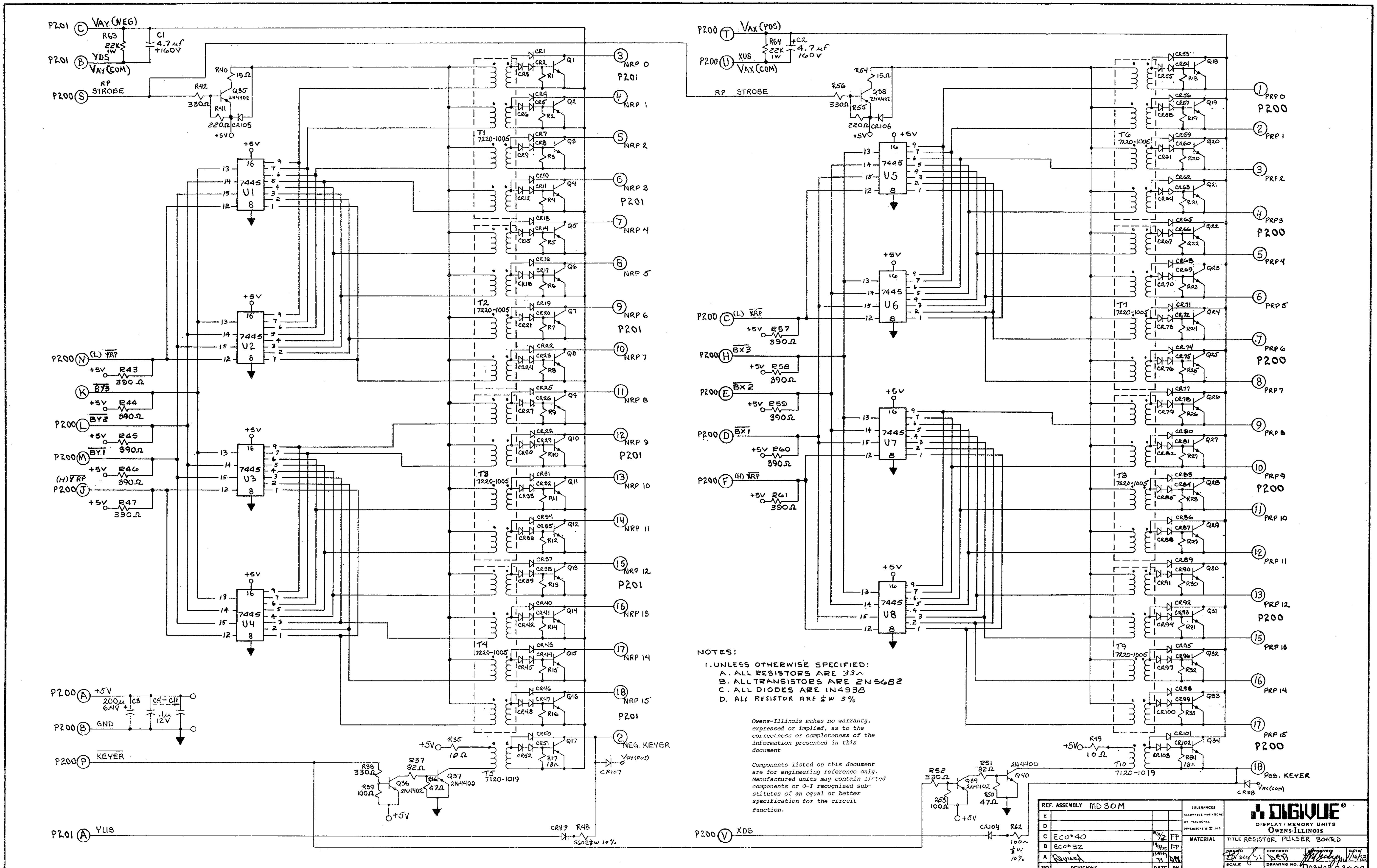
Schematics and assembly drawings for the display printed circuit boards are provided in the following pages. Parts lists are included on each assembly drawing. A drawing of the inaccessible side of the motherboard is provided for convenience in tracing printed conductors on that board.


Timing Slot
0
5
10
15
20
25
30
$\overline{YU'}$
$\overline{YM}$
$\overline{XDB}$
$\overline{XUB}$
$\overline{YDB}$
$\overline{YUB}$
$\overline{XD°}$
$\overline{XD'}$
$\overline{XU°}$
$\overline{XU'}$
$\overline{XM}$
$\overline{YD°}$
$\overline{YD'}$
$\overline{YU°}$
SWEB
Timing Slot
0
5
10
15
20
25
30
$\overline{RP\ STROBE}$
$\overline{DS\ STROBE}$
$\overline{KEYER}$
STATUS
SYNC
SBWE
SWEB
S-Sustain W-Write E-Erase B-Bulk Erase
LO HI

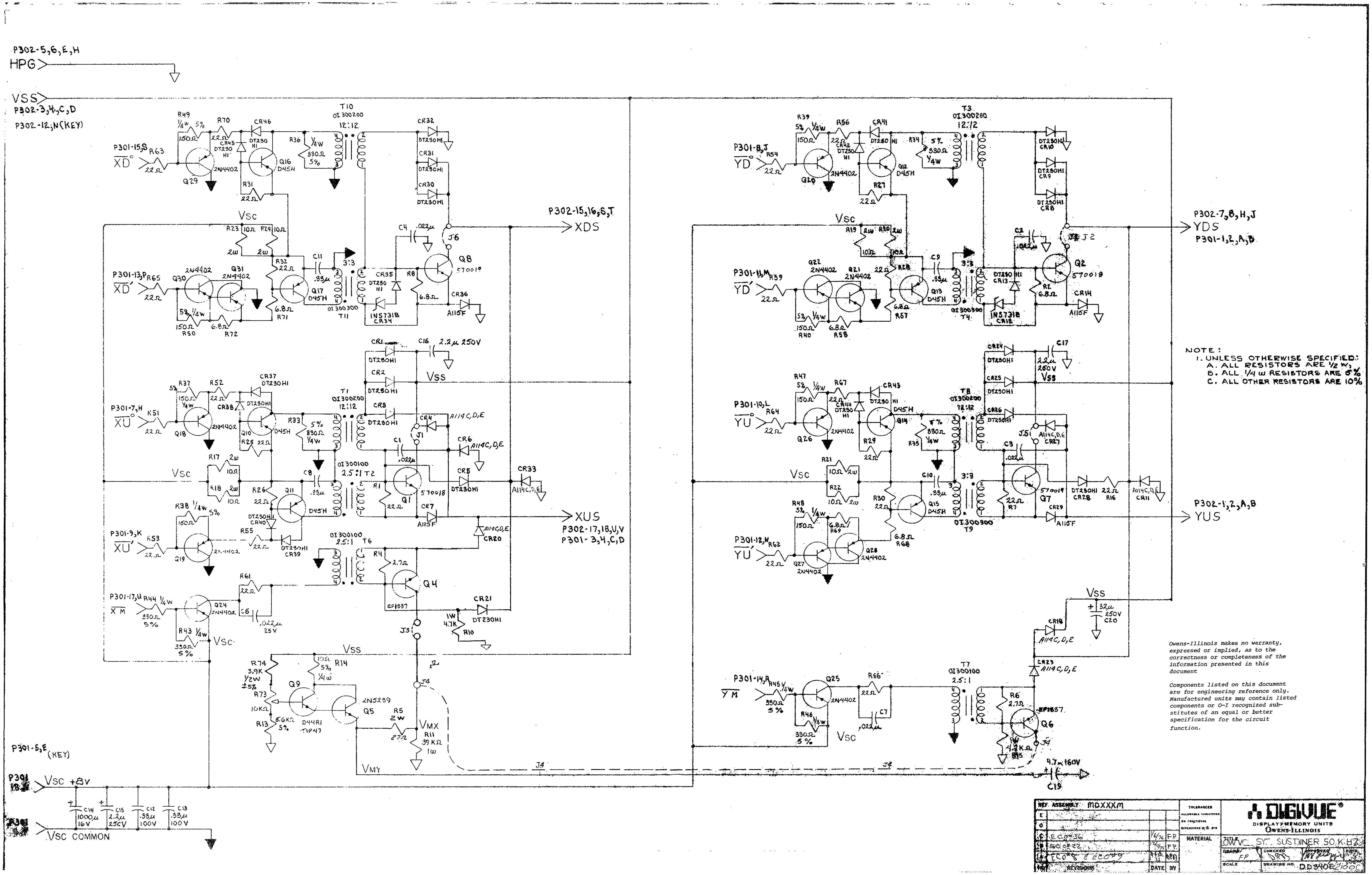

Timing Slot 0 5 10 15 20 25 30
Pin 1
2
3
4
5
6
7
9
ROM 4I - UI7
BULK OPERATION
ROM 42 - U33
WRITE & SUSTAIN
OPERATIONS
ROM 42 - U33
ERASE OPERATION
ROM 43A - UI8
ERASE OPERATION
ROM 44A - UI9
BULK OPERATION
ROM 45 - U34
WRITE & SUSTAIN
OPERATIONS
■ LO □ HI



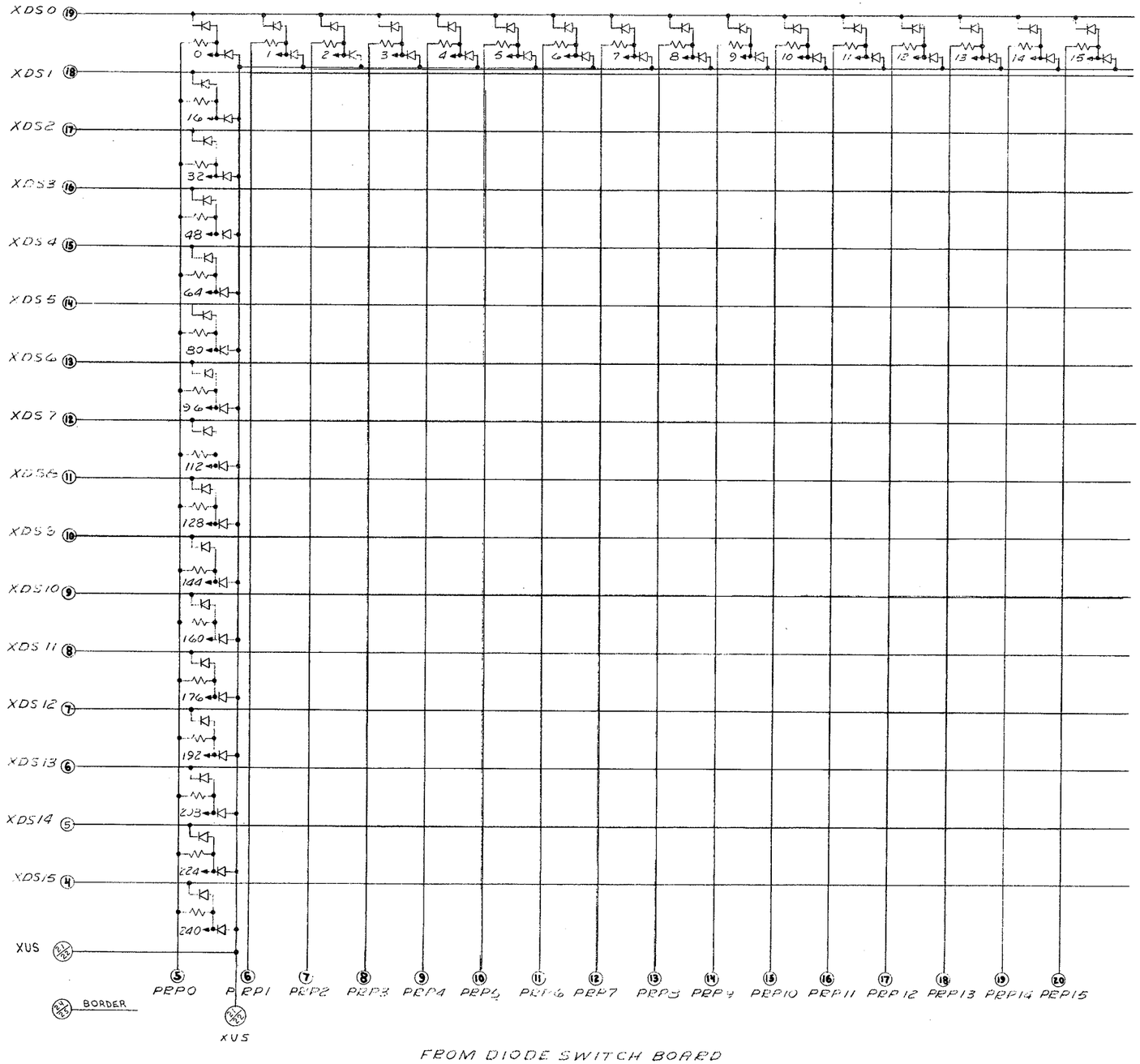
Note: All unmarked resistors ARE 1.0 KΩ in 16 pin packs
COMPONENT SIDE P.C.B. 100A
P100
P101
P102
SYMBOL
Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document.
Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.
WRITE
ERASE
BULK ERASE
STATUS
SYNC
RP STROBE
KEYER
STROBE
50KC
LOAD
DS800T
DS900
DS800B
DS1000
CHASSIS GND
Vcc
GND
G ECO#44 3/22/? FP
F EC.O#41 3/8/76 FP
REF. ASSEMBLY
E ECO#31 11/11/75 FP
D ECO#31 10/24/75 FP
C ECO#28 7/31/75 FP
B ECO#27 7/15/75 FP
A ECO#21 6/11/75 FP
H ECO#43 4-31-76 DPB
NO REVISIONS DATE BY
TOLERANCES
MATERIAL
DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS
TITLE LOW VOL. SYS. LOGIC 5 ROM 50 KHZ
DRAWN
CHECKED
APPROVED
DATE 5/30/74
SCALE
DRAWING NO. DD340E2000H



P201 C VAY (NEG)
P201 B YDS VAY (COM)
P200 S RP STROBE
R63 22K 1W
C1 4.7 uf +160V
7445 U1
7445 U2
7445 U3
7445 U4
T1 7220-1005
T2 7220-1005
T3 7220-1005
T4 7220-1005
T5 7120-1019
NRP 0
NRP 1
NRP 2
NRP 3
NRP 4
NRP 5
NRP 6
NRP 7
NRP 8
NRP 9
NRP 10
NRP 11
NRP 12
NRP 13
NRP 14
NRP 15
NEG. KEYER
P201
P200 N (L) YRP
K BY3
P200 L BY2
P200 M BY1
(H) YRP P200 J
P200 A +5V
P200 B GND
P200 P KEYER
P201 A YUS
P200 T VAX (POS)
P200 U XUS VAX (COM)
R64 22K 1W
C2 4.7 uf 160V
RP STROBE
7445 U5
7445 U6
7445 U7
7445 U8
T6 7220-1005
T7 7220-1005
T8 7220-1005
T9 7220-1005
T10 7120-1019
P200 C (L) XRP
P200 H BX3
P200 E BX2
P200 D BX1
P200 F (H) XRP
PRP 0
PRP 1
PRP 2
PRP 3
PRP 4
PRP 5
PRP 6
PRP 7
PRP 8
PRP 9
PRP 10
PRP 11
PRP 12
PRP 13
PRP 14
PRP 15
POS. KEYER
P200
P200 V XDS
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 33Ω
B. ALL TRANSISTORS ARE 2N5682
C. ALL DIODES ARE 1N4938
D. ALL RESISTOR ARE 1/4W 5%
Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document
Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.
REF. ASSEMBLY MD30M
C ECO#40
B ECO#32
A Revised
NO REVISIONS DATE BY
MATERIAL
DIGIVUE
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS
TITLE RESISTOR PULSER BOARD
DRAWING NO. D0340E0200C


P302-5,6,E,H
HPG
VSS
P302-3,4,C,D
P302-12,N(KEY)
P301-15,S
XD
P301-13,P
XD'
P301-7,H
XU
P301-9,K
XU'
P301-17,U
XM
P302-15,16,S,T
XDS
P302-17,18,U,V
P301-3,4,C,D
XUS
P301-8,J
YD
P301-11,M
YD'
P301-10,L
YU
P301-12,N
YU'
P301-14,R
YM
P302-7,8,H,J
YDS
P301-1,2,A,B
P302-1,2,A,B
YUS
P301-5,E (KEY)
Vsc +8V
Vsc COMMON
VMX
VMY
NOTE:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 1/2 W,
B. ALL 1/4 W RESISTORS ARE 5%
C. ALL OTHER RESISTORS ARE 10%
Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document
Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.
REF. ASSEMBLY MDXXXM
ECO436 1/6/76 FP
ECO422 12/11/75 FP
ECO8 & ECO9
REVISIONS DATE BY
TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010
MATERIAL
DIGIVUE
DISPLAY/MEMORY UNITS
OWENS-ILLINOIS
TITLE LOW VC. SY. SUSTAINER 50 K HZ
DRAWN FP
CHECKED
APPROVED
DATE
SCALE
DRAWING NO. DD3406 2100C

FROM DIODE SWITCH BOARD
CONNECTOR P401



FROM DIODE SWITCH BOARD
CONNECTOR P400

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE 5.6K
   B. " " " 1/4W
   C. " DIODES ARE 1N4938 OR ITT2002

NO	REVISIONS	DATE	BY
E			
D			
C			
B	ECO#14	3/14/75	FP
A	Revised	10/17/74	TH

TOLERANCES ILLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010
MATERIAL

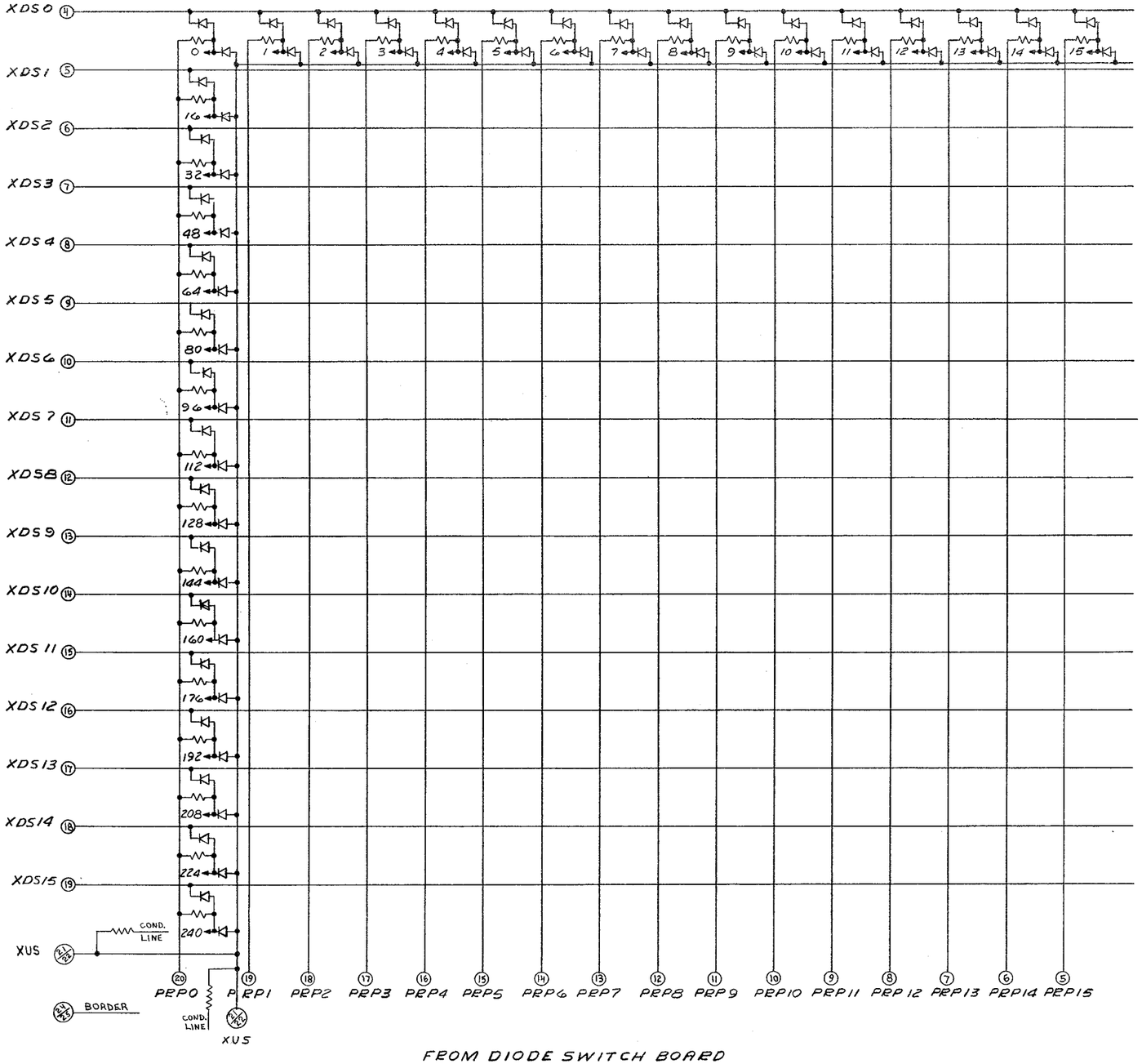
DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS

TITLE MATRIX × EVEN

DRAWN	CHECKED	APPROVED	DATE
J Diller			10-17-74

SCALE
DRAWING NO. DD3402400B

FROM DIODE SWITCH BOARD
CONNECTOR P501



FROM DIODE SWITCH BOARD
CONNECTOR P500

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE 5.6K
   B. " " " 1/4 W
   C. " DIODES ARE IN4938 OR ITT2002

REF. ASSEMBLY			
E			
D			
C			
B			
A	Revised	10 Nov 74	WB
NO	REVISIONS	DATE	BY

TOLERANCES: ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010
MATERIAL

DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS

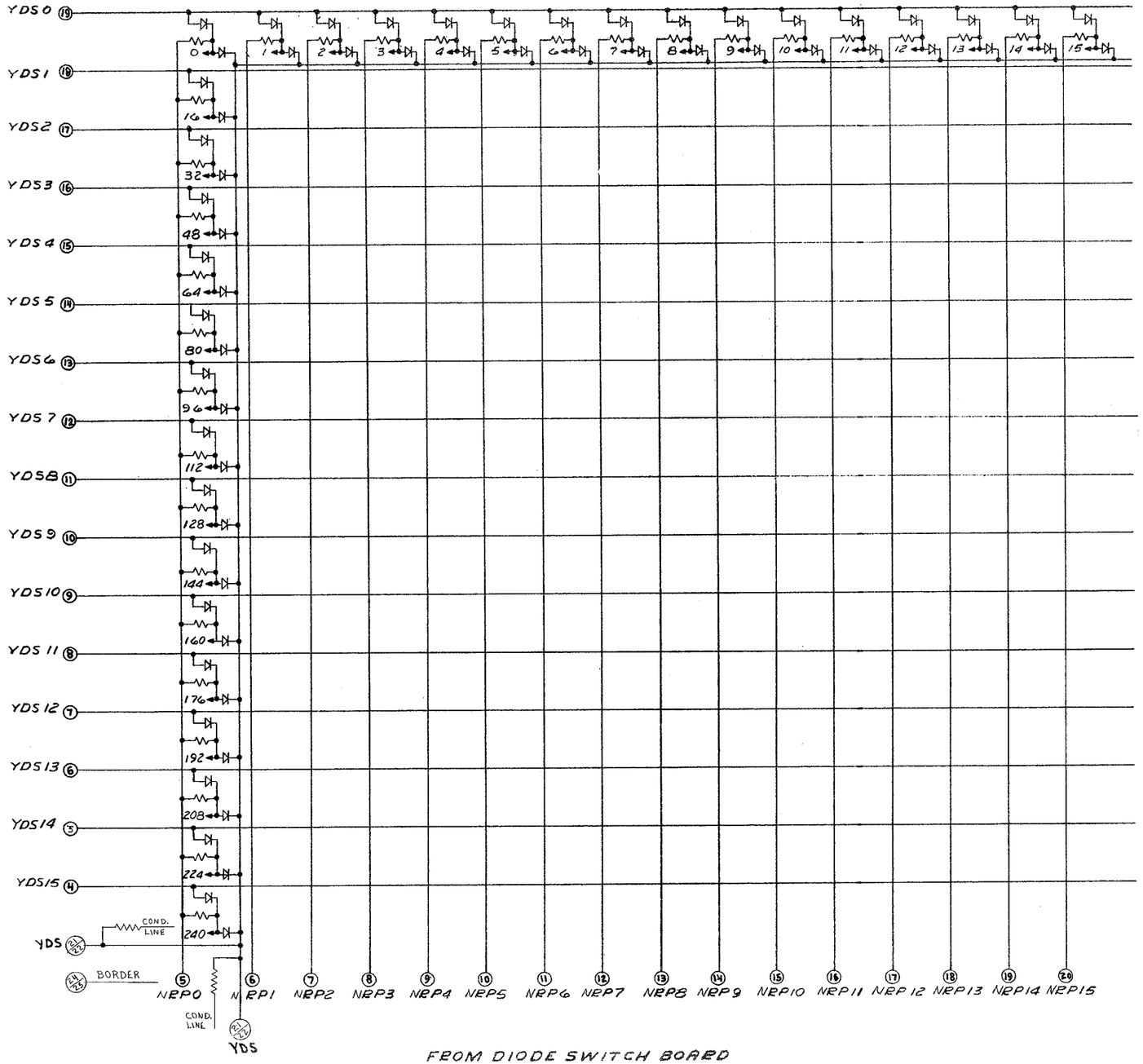
TITLE MATRIX X ODD

DRAWN	CHECKED	APPROVED	DATE
J Dillon	DEO		

SCALE

DRAWING NO DD 340E0500A

FROM DIODE SWITCH BOARD
CONNECTOR P-601



FROM DIODE SWITCH BOARD
CONNECTOR P-600

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE 5.6 K
   B. " " " 1/4 W
   C. " DIODES ARE IN4938 OR ITT2002

REF. ASSEMBLY			
E			
D			
C			
B			
A	Revised	10-31	NRB
NO	REVISIONS	DATE	BY

TOLERANCES
ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010
MATERIAL

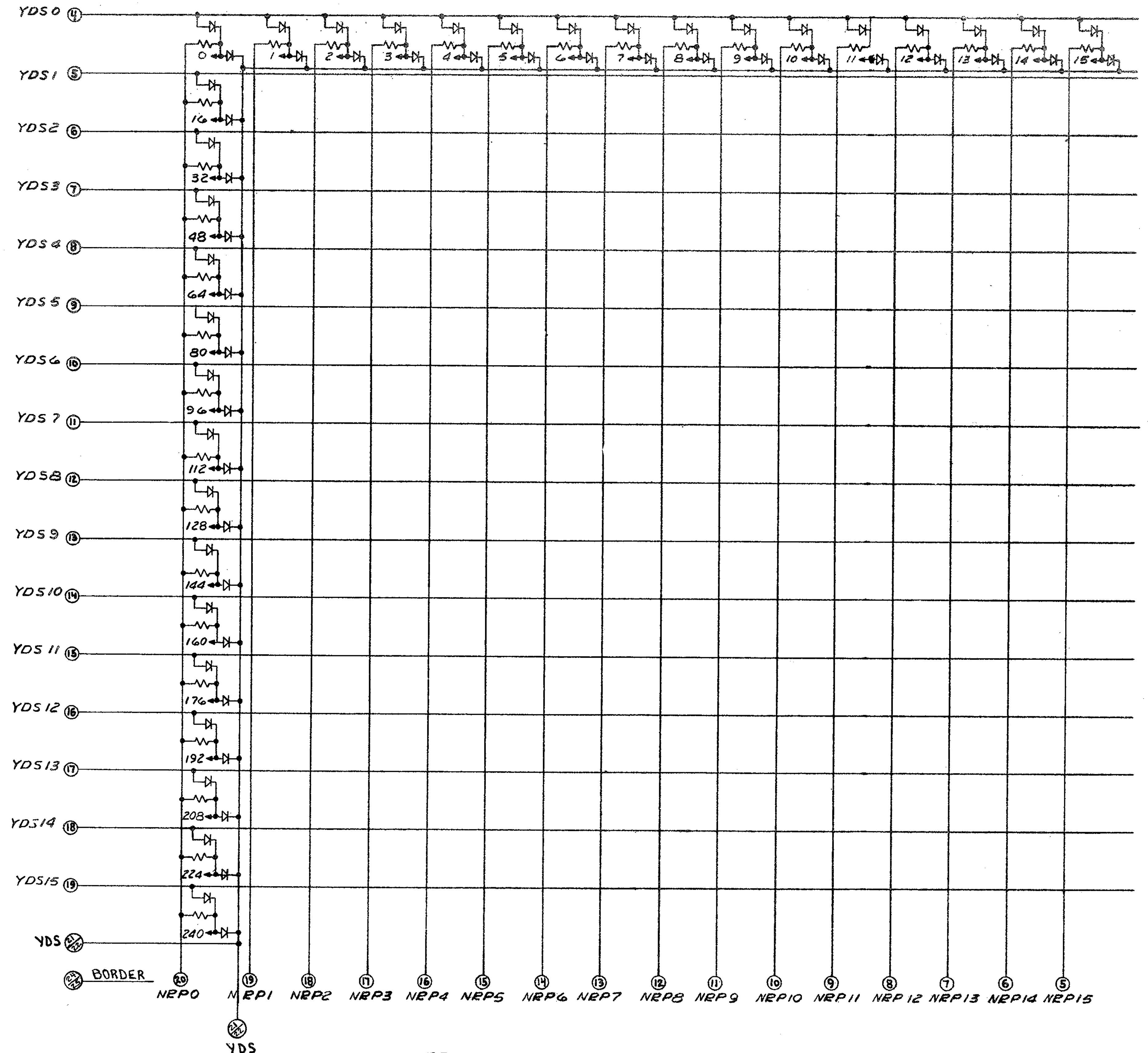
DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS

TITLE MATRIX Y ODD

DRAWN	CHECKED	APPROVED	DATE
J. Miller			12-7

SCALE
DRAWING NO. DD3486E0600A

FROM DIODE SWITCH BOARD
CONNECTOR P-701



FROM DIODE SWITCH BOARD
CONNECTOR P-700

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 5.6K
B. " " " 1/4 W
C. " DIODES ARE 1N4938 OR ITT2002

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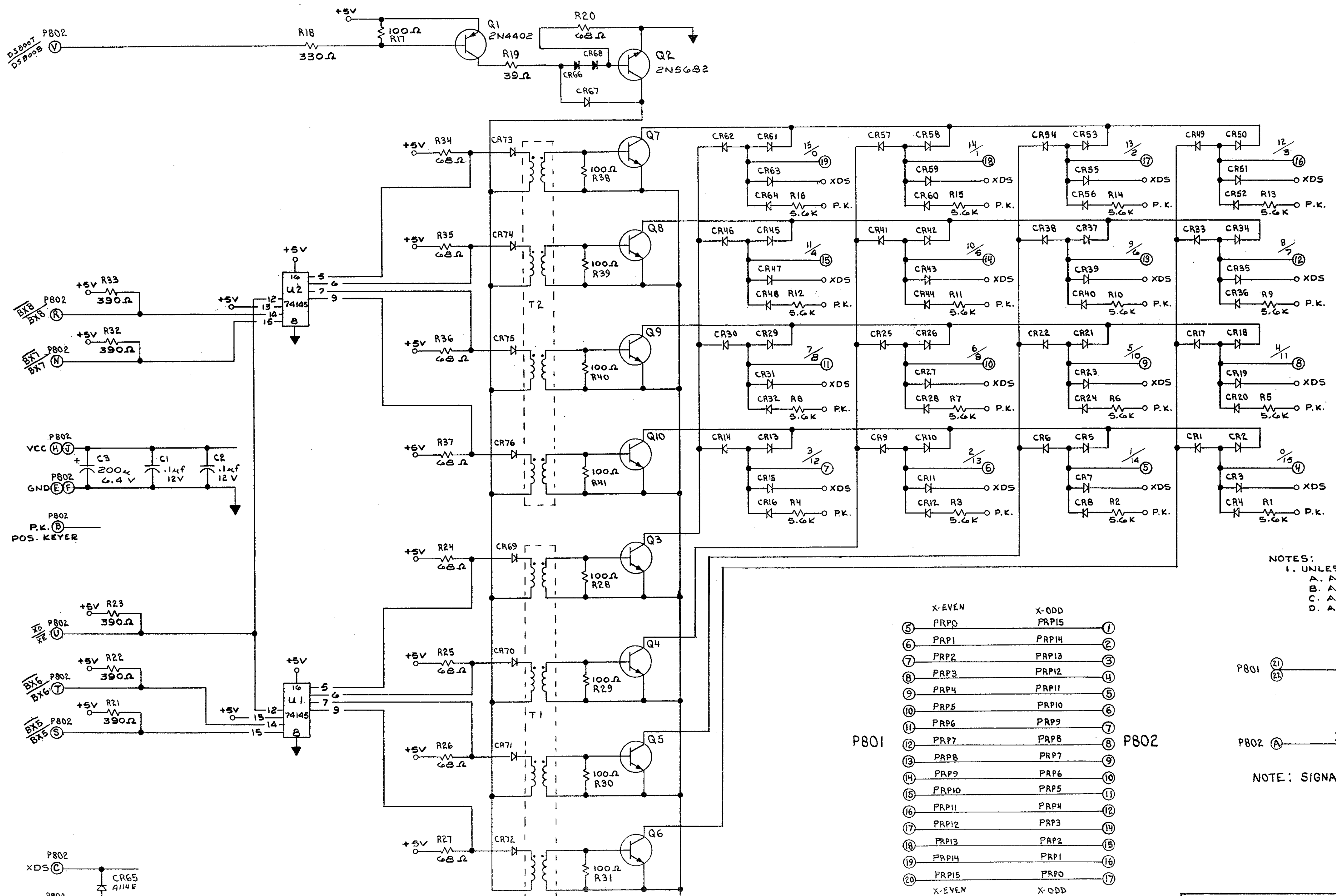
Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.

REF. ASSEMBLY				TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS ± .015	DIGIVUE DISPLAY / MEMORY PANEL Owens-Illinois
E					
D					
C				MATERIAL	TITLE MATRIX [illegible]
B	ECO#14	[illegible]	FP		
A	[illegible]				
NO	REVISION	DATE	BY		

Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document.

Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.



NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   A. ALL RESISTORS ARE 1/4W, 5%
   B. ALL TRANSISTORS ARE 2N5551
   C. ALL DIODES ARE 1N4938 OR ITT2002
   D. ALL TRANSFORMERS ARE 7220-1005

P801 / P802

P801	X-EVEN	X-ODD	P802
5	PRP0	PRP15	1
6	PRP1	PRP14	2
7	PRP2	PRP13	3
8	PRP3	PRP12	4
9	PRP4	PRP11	5
10	PRP5	PRP10	6
11	PRP6	PRP9	7
12	PRP7	PRP8	8
13	PRP8	PRP7	9
14	PRP9	PRP6	10
15	PRP10	PRP5	11
16	PRP11	PRP4	12
17	PRP12	PRP3	14
18	PRP13	PRP2	15
19	PRP14	PRP1	16
20	PRP15	PRP0	17
	X-EVEN	X-ODD	

P801 (21)(22) — XUS — (21)(22) P800

P802 (A) — X BORDER — (24)(20) P800

NOTE: SIGNALS TO 800 BOARDS → X-ODD / X-EVEN

NO	REVISIONS	DATE	BY
E			
D			
C	ECO# 32	10/3/75	FP
B	Revised	6/26/74	DPB
A	Revised	15 Mar 74	DPB

REF. ASSEMBLY

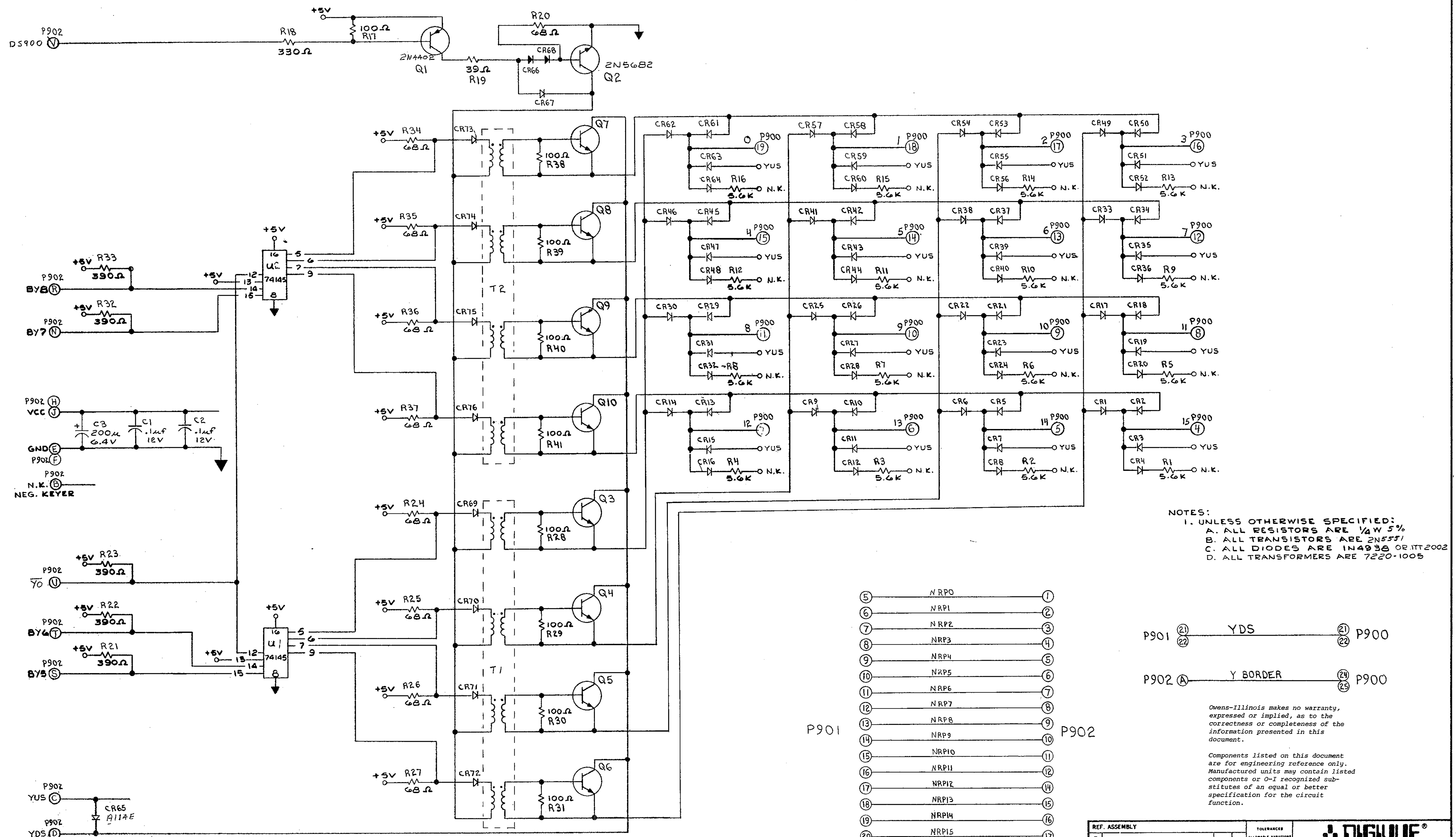
TOLERANCES

MATERIAL

DIGIVUE® DISPLAY / MEMORY UNITS Owens-Illinois

TITLE: X EVEN + ODD DIODE SWITCH

DRAWING NO. DD340E0800



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   - A. ALL RESISTORS ARE 1/4W 5%
   - B. ALL TRANSISTORS ARE 2N5551
   - C. ALL DIODES ARE 1N4938 OR ITT2002
   - D. ALL TRANSFORMERS ARE 7220-1005

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Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.

NO	REVISIONS	DATE	BY
E			
D			
C	ECO#32	9/12/75	EP
B	Revised ECO # 13	16 Jul 74	WPB
A	Revised	19 Feb 74	WPB

REF. ASSEMBLY

TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

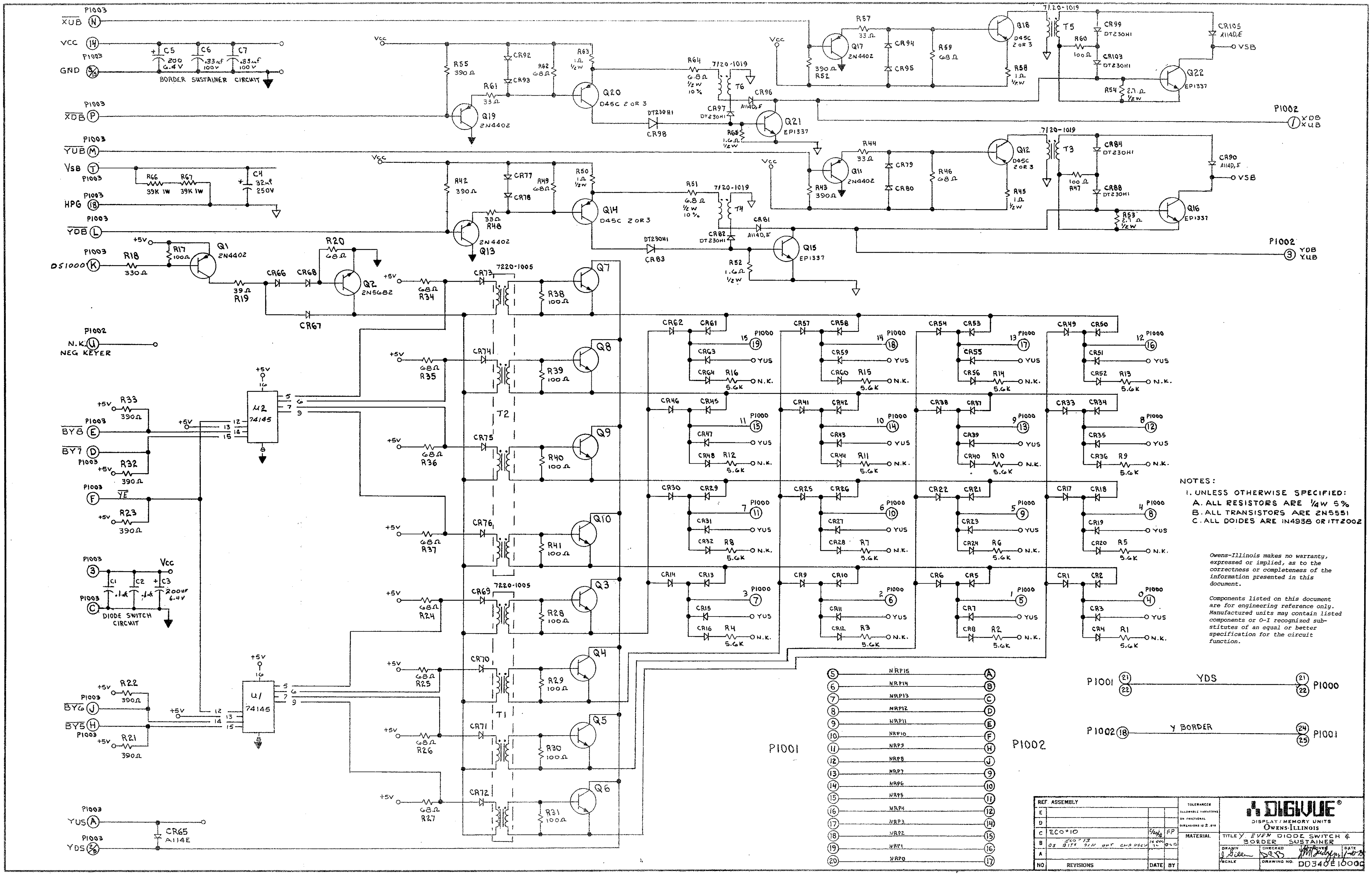
MATERIAL

DIGIVUE® DISPLAY / MEMORY UNITS OWENS-ILLINOIS

TITLE Y-ODD DIODE SWITCH

DRAWN J. Gillen | CHECKED DPB | APPROVED | DATE 8-74

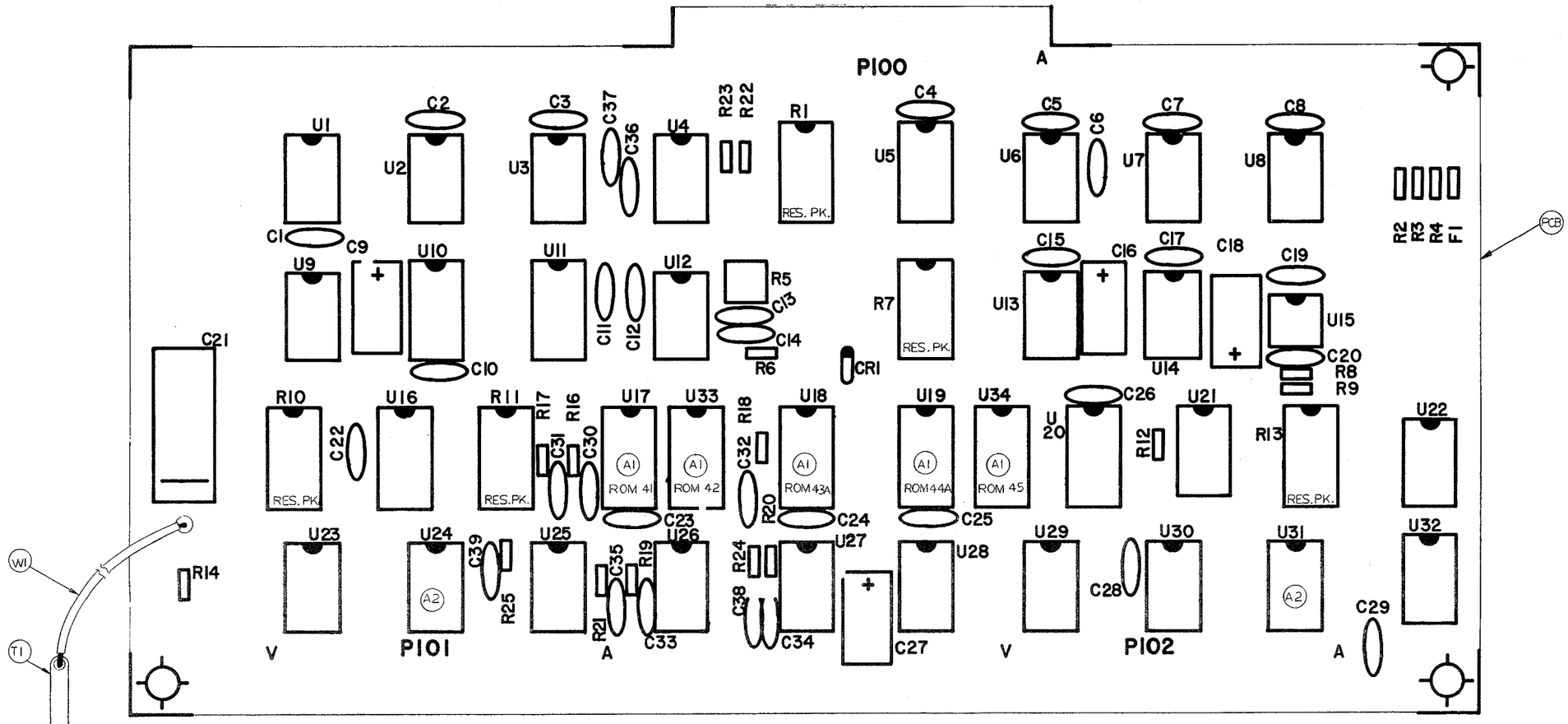
SCALE | DRAWING NO. DD340E09000



BORDER SUSTAINER CIRCUIT
DIODE SWITCH CIRCUIT
P1003
XUB
VCC
GND
XDB
YUB
VSB
HPG
YDB
DS1000
N.K.
NEG KEYER
BY8
BY7
YE
BY6
BY5
YUS
YDS
P1002
XDB XUB
YDB YUB
P1000
P1001
YDS
Y BORDER
7120-1019
7220-1005
74145
2N4402
2N5682
D45C 2 OR 3
EP1337
DT230H1
A114D,E
A114E
NRP15
NRP14
NRP13
NRP12
NRP11
NRP10
NRP9
NRP8
NRP7
NRP6
NRP5
NRP4
NRP3
NRP2
NRP1
NRP0
NOTES:
1. UNLESS OTHERWISE SPECIFIED:
A. ALL RESISTORS ARE 1/4W 5%
B. ALL TRANSISTORS ARE 2N5551
C. ALL DOIDES ARE IN4938 OR ITT2002
Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document.
Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.
REF ASSEMBLY
C ECO #10
B ECO #13 DS BITS 9/11 OUT CHANGED
NO REVISIONS DATE BY
TOLERANCES
MATERIAL
DIGIVUE
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS
TITLE Y EVEN DIODE SWITCH & BORDER SUSTAINER
DRAWN
CHECKED
APPROVED
DATE
SCALE
DRAWING NO. D0340E1000C

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
PCB	1	PRINTED CIRCUIT BRD		DD340D0100 I
U1,7,32	3	I.C. 7412	T.I.	SN7412
U2,4	2	" 7404	"	SN7404
U3,22	2	" 7400	"	SN7400
U5	1	" 74155	"	SN74155
U6	1	" 7474	"	SN7474
U8	1	" 7493	"	SN7493
U9,13,14,25-28,31	8	" 7417	"	SN7417
U10,11	2	" 74161	"	SN74161
U12	1	" 74122	"	SN74122
U15	1	" NE555	SIGNETICS	NE555V
U16,20	2	" 74156	T.I.	SN74156
U21,23,24,29,30	5	" 7416	"	SN7416
U17,18,19,33,34	5	ROMS 41,42,43A,44A,45	INTERSIL	IM5600
R1,7,10,11,13	5	RESISTOR 1K.	CTS	CTS15R-1K
R 2-4	3	" .25W 1K. 10%	A.B.	RCR07
				TYPE C4
R8	1	" " 100K 5%	A.B.	RCR07
R9	1	" " 390K "	"	"
R12	1	" " 100Ω "	"	"

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
R14	1	RESISTOR .25W 12K 10%	A.B.	RCR07
R5	1	POTENTIOMETER 2K	CTS	CTS362U202B
R16-25	10	RESISTOR .25 W 390Ω 5%	A.B.	RCR07
C30 - 39	10	CAPACITOR 100PF@ 1000V	CENTRALAB	DD-101
C1-5,7,8,10,11,13,17,19,20	20	" .1UF@ 12V	"	XXUK-12-104
C22-26,28,29		" " "	"	"
C6,15	2	" 220PF@ 500V	"	CE221
C9,16,18,27	4	" 22UUF@ 10V	IEC	TAD220TH10
C12	1	" 500 PF@500V	ERIE	831-000-X5F0-501K
C21	1	" 2.2UF@ 250V	MEPCO	C280MAE/A2M2
C14	1	" 220PF@50V NPO 5%	CENTRALAB	CN15C221J
CR1	1	DIODE	T.I.	IN4938
F1	1	FUSE .375 AMP N.B.	LITTLE FUSE	275.375
A1	5	SOCKET I.C. 16 PIN	AUGAT	316-AG5-D2R
A2	2	" " 14 PIN	"	314-AG5-D2R
W1	1	3½" 18 AWG, UL STYLE 1007, 300V, 80°C, BLACK, PRE-TINNED		
T1	1	SOLDER. LUG #6	ZERICK	501-6
R6	1	RESISTOR .25W 6.2K 2%	CORNING	TYPE C4 (USE WITH 270073)
		" " 4.7K "	"	" " (USE WITH 270074)



Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document.

Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.

NO	REVISIONS	DATE	BY
H			
G	ECO#41	3/19/76	FP
F	ECO#31	11/6/75	FP
REF. ASSEMBLY			
E	ECO#31	10/24/75	FP
D	ECO#32	10/24/75	FP
C	ECO#28	7/6/75	FP
B	ECO#27	7/5/75	FP
A	ECO#21	6/19/75	FP

TOLERANCES: ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL

DIGIVUE®
DISPLAY/MEMORY UNITS
OWENS-ILLINOIS 10-30-75

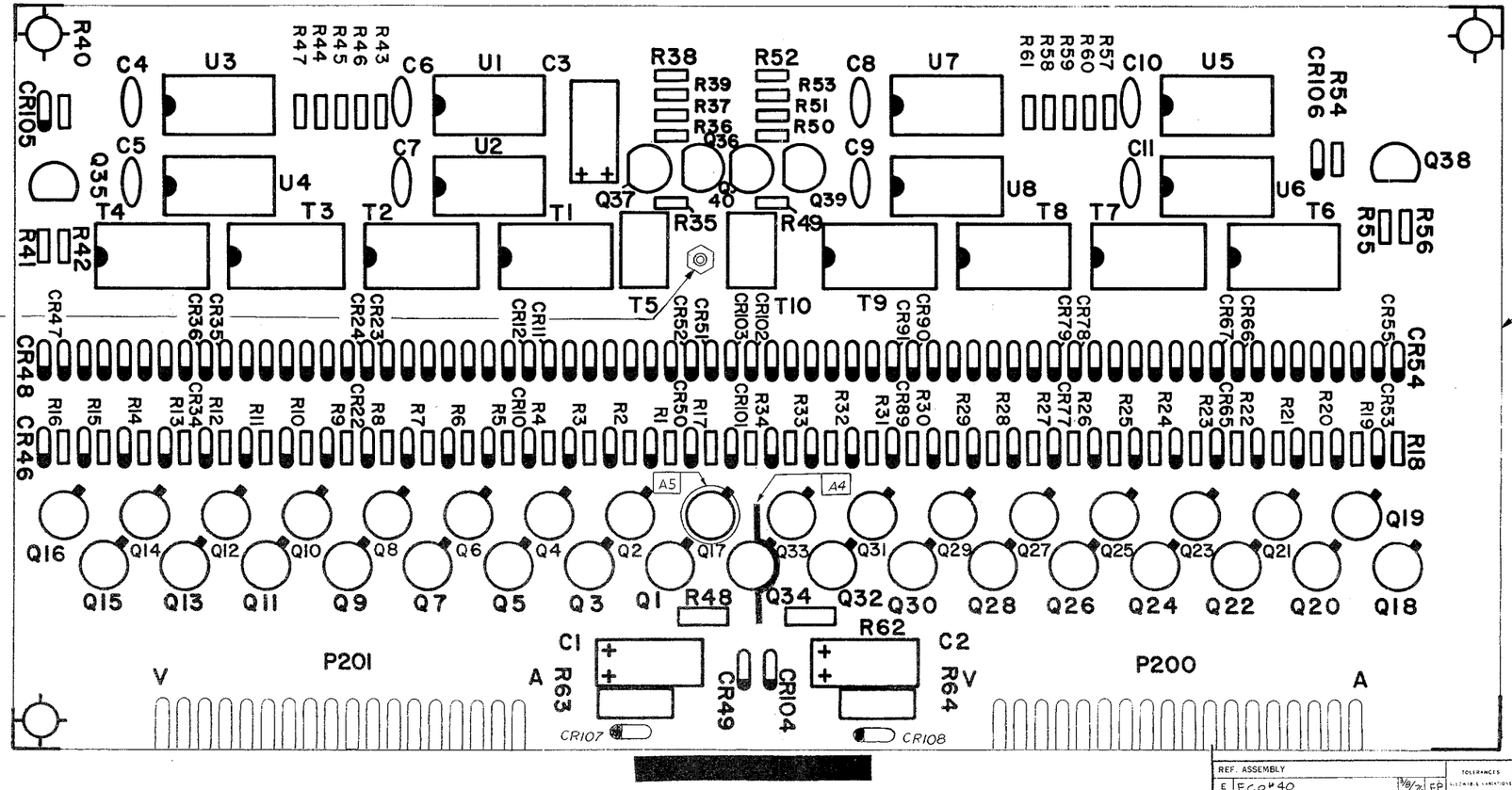
TITLE: LOW VOL. SYS. LOGIC 5 ROM 50 KHZ

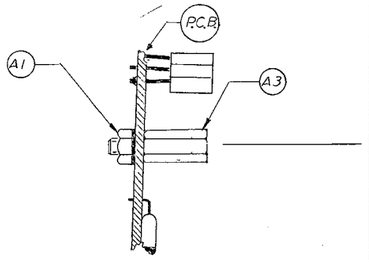
DRAWN: FP | CHECKED | APPROVED | DATE

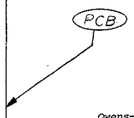
SCALE 2:1 | DRAWING NO. DD340C2000G

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
C1, C2	2	CAP 6.4 uf 15v	MEPCO	C436AP/K6.4
C3	1	" 220uf at 10v	I.E.C.	TAD220THIO
C4 - C11	8	" .1uf at 10v	CENTRALAB	XXUKI2-104
CR1 - CR104	96	DIODE		IN4938 or ITT2002
Q1 - Q34	34	TRANSISTOR 2N5682	MOTOROLA/FAIR.	2N5682
Q35,36,38,39	4	" 2N4402	" "	2N4402
Q37,40	2	" 2N4400	" "	2N4400
R17, 34	2	RESISTOR .25W 18Ω 5%	A.B.	RCR07
R1-16 R18-33	32	" " 33Ω "	"	"
R40, 54	2	" " 15Ω "	"	"
R36, 50	2	" " 47Ω "	"	"
R37, 51	2	" " 82Ω "	"	"
R38,42,52,56	4	" " 330Ω "	"	"
R39, 53	2	" " 100Ω "	"	"
R41, 55	2	" " 220Ω "	"	"
R43-47, 57-61	10	" " 390Ω "	"	"
R35, 49	2	" " 10Ω "	"	"

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
R62	1	RESISTOR .5W 100Ω 10%	A.B.	RCR20
R63,64	2	" 1W 22K 10%	"	RCR32
R48	1	" .5W 560Ω 10%	"	RCR20
U1 - U8	8	I.C. 7445	T.I.	SN7445
T1 - T4 T6 - T9	8	TRANSFORMER	POTTER	7220-1005
T5, T10	2	"	"	7120-1019
A1	1		SHAKEPROOF	511-061800-00 ZINC PLATE
A3	1	STANDOFF	POSITRONICS	14H5-06-X8F ZINC PLATE
A4	1	HEAT SINK	WAKEFIELD	296-2-AB
PCB	1	PRINTED CIRCUIT BD.		CD340D0200
A5	1	HEAT SINK	THERMALLOY	1115B







Note #

1. Zinc Plating per Zinc Dichromate Spec 210M0200A Type II, Class 2

2. See General Purchased Component Requirements 220M0300.

NO	REVISIONS	DATE	BY
E	ECO #40	7/8/76	FP
D	ECO #32	4/14/76	FP
C	Revised ECO #24	4/4/75	MRA
B	Revised per ECO #17	3/11/75	MRA
A	Revised per Pre-Production	3/13/74	FP

REF. ASSEMBLY

TOLERANCES

MATERIAL

DIGIVUE®
DISPLAY MEMORY UNITS
OWENS-ILLINOIS

TITLE COMPONENT ASSEMBLY

DRAWN	CHECKED	APPROVED	DATE
EBM	JSB	JCM	6/74

SCALE 2X

DRAWING NO. DD340C0200E

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
C1 -6,7		CAP .022uf@25V	CENTRALAB	UK25-E23
C8-13	6	" .33uf@100V	I.E.C.	MDEF334MBIA
C14	1	" 1000uf@16V	MEPCO	ET102X016A02
C15-17	3	" 2.2uf@250V	"	C280MAE/A2M2
C19	1	" 6.4 uf@ 150V	"	C436AR/M6.4
C20	1	" 32uf@ 250V	"	C436AR/M32
CR4,6,11,18,20,23,27,33	8	DIODE	GE.	A114C
CR1-3,5,8-10,13,21,24	27	"	"	DT230H1
CR25,28,30-32,35,37-46		"	"	
CR7,14,29,36	4	"	GE.	A115F
CR12,34	2	"	MEPCO	IN5231B
Q18-22,24-31	13	TRANSISTOR	MOT./FAIR.	2N4402
Q7, 8	2	"	KERTRON/SOLITRON	570019
Q1,2	2	"	" "	570018
Q4,6	2	"	T.I.	EP1337
Q5	1	"	RCA	2N5239
Q9	1	"	T.I.	TIP47
Q10-17	8	"	G.E.	D45H1
PCB	1	PRINTED CKT. BOARD		DD340D0300
A1	1	HEAT SINK		BD340M2500B
A2	17	4-40 THREADED BUSH.	USECO	90040B-NS PLATED
A3	14	4-40X.500 PAN HD. SCREW	- ZINC PLATED	
	1			
J4	1	WIRE, 18AWG, 4" BLACK		

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
R14	1	RESISTOR .25W 10% 5%	A.B.	RCR07
R33-36,43-46	8	" " 330Ω "	"	"
R37-40,47-50	8	" " 150Ω "	"	"
R13	1	" .5W 5.6K "	"	RCR20
R74	1	" " 3.9K "	"	"
R4,6	2	RESISTOR .5W 2.7Ω 10%	A.B.	RCR20
R1,7,16,25-32,51-56,59	26	" " 22Ω "	"	"
R61-67,70	8	" " " "	"	"
R2, 8, 57,58,68,69,71,72	8	" " 6.8Ω "	"	"
R10,15	2	" 1W 4.7K "	"	RCR32
R11	1	" " 39K "	"	"
R17-24	8	" 2W 10Ω "	"	RCR42
R5	1	" " 27Ω "	"	"
R73	1	POT. 1W 10K	BOURNS	3345-W-1-103-10K
T1,3,8,10	4	TRANSFORMER 12:12	PULSE ENGIN.	Q1.300200
T2, 6,7	3	" 25:1	" "	Q1.300100
T4,9,11	3	" 3:3	" "	Q1.300300
A5	7	KAPTON INSULATOR	THERMALLOY	43-03-9
A6	4	SCREW 6-32X.375PanHd	- ZINC PLATE	
J1-3,5,6	5	WIRE, 18AWG, 3" BLACK	PRE-FUSED	UL STYLE 1007
A7	2	LEAD SPACER	ROBINSON ELEC.	RC-T03062-1
A4	1	HEAT SINK SUPPORT		BD340M3800
A8	1	4-40 X.250 PAN HD. SCREW		ZINC PLATE
A9	15	LOCKWASHER, INT. TH. #4		ZINC PLATE

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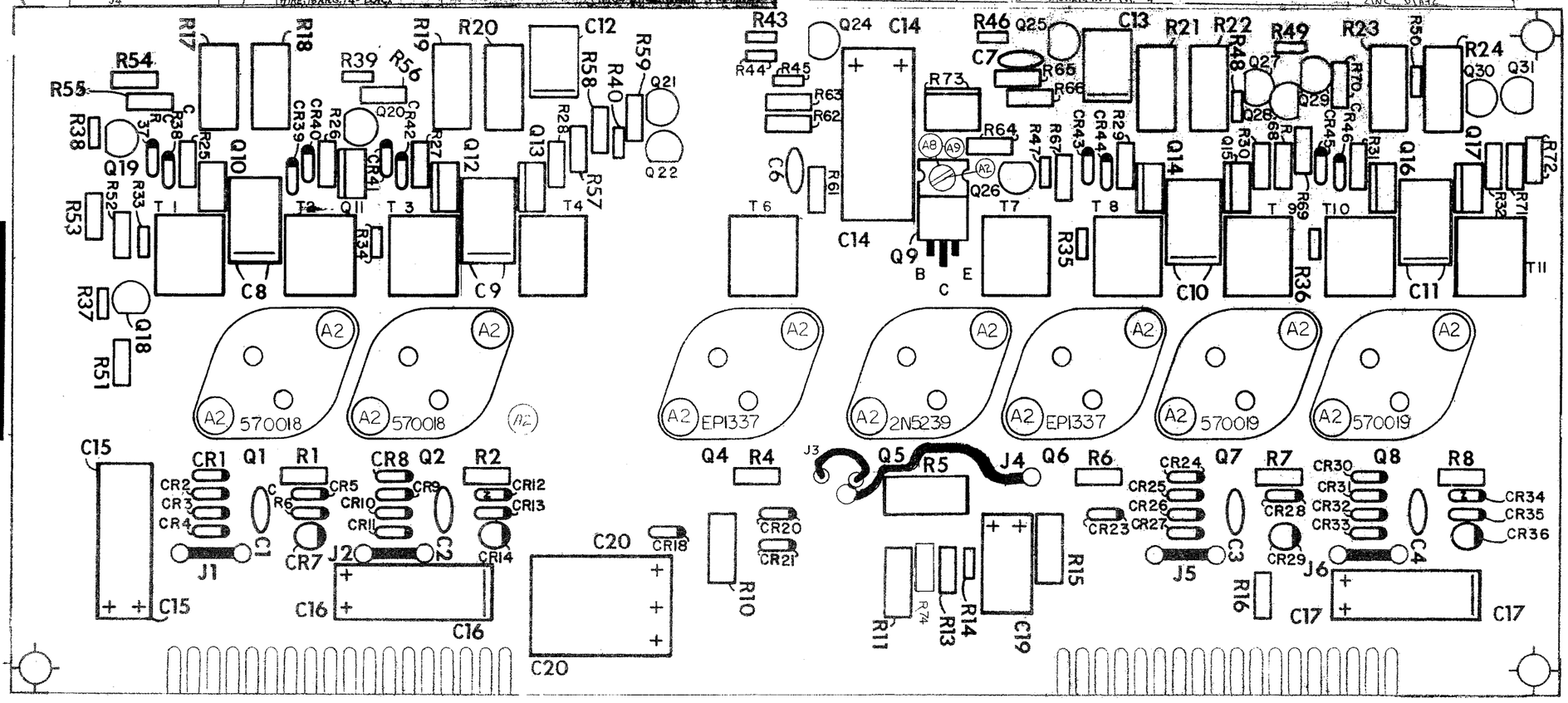
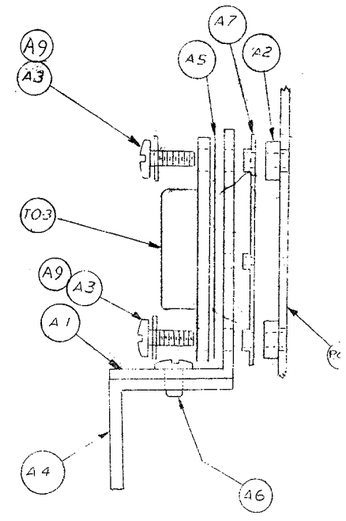
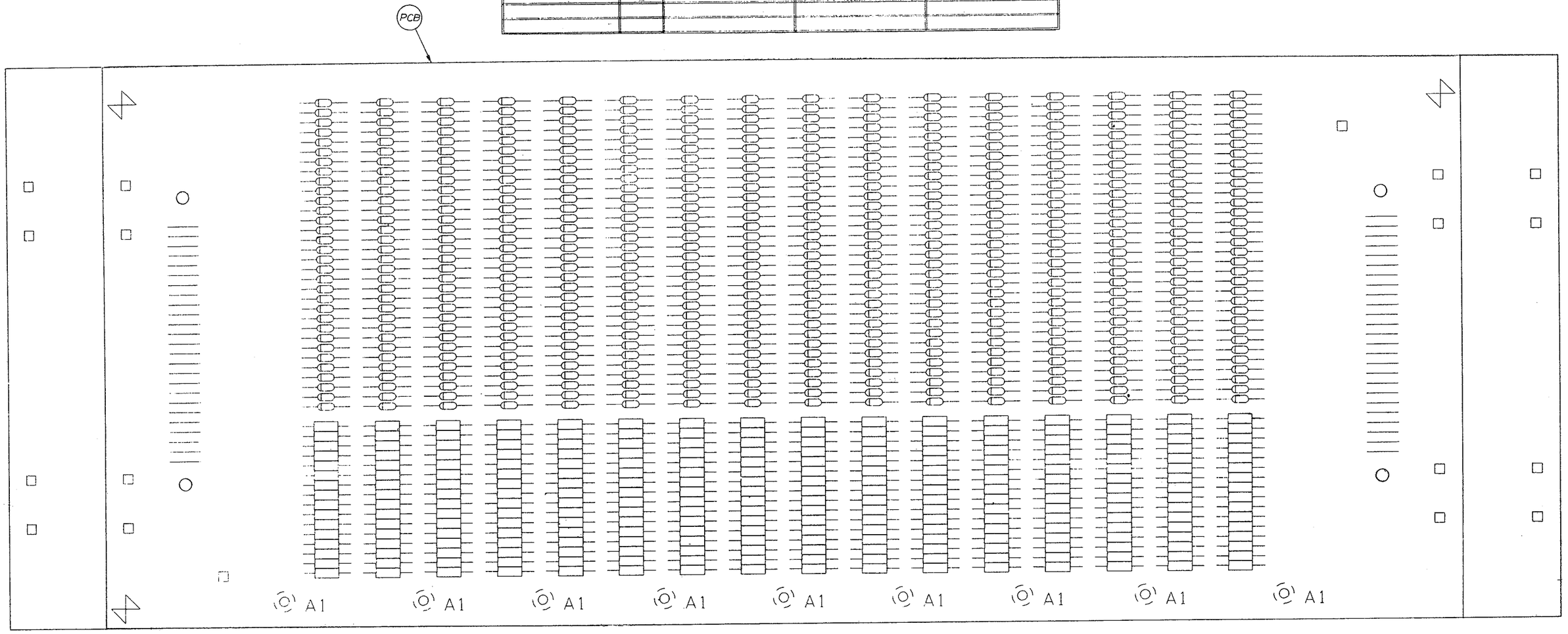
P.C.B.





REF. ASSEMBLY MDXXXM				TOLERANCES	DIGIVUE® DISPLAY MEMORY UNITS OWENS-ILLINOIS
E					
D	ECO#36	3/4/74	FP		
C	ECO#22	12/11/73	FP	MATERIAL	SUSTAINER 50 KHZ
B	ECO# 25 & 24				
A	ECO# [illegible]				
NO	REVISIONS	DATE	BY	SCALE 2X	DRAWING NO. 003402100

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
UNM'K	512	DIODE		IN4938/ITT2002
UNM'K	256	RES.25W 5.6K 10%	A.B.	RCR07
PCB	1	PRINTED CKT. BRD.		CD340D0400E
A1	9	2-56 THD. BUSH.	PEM	Y-1316ET



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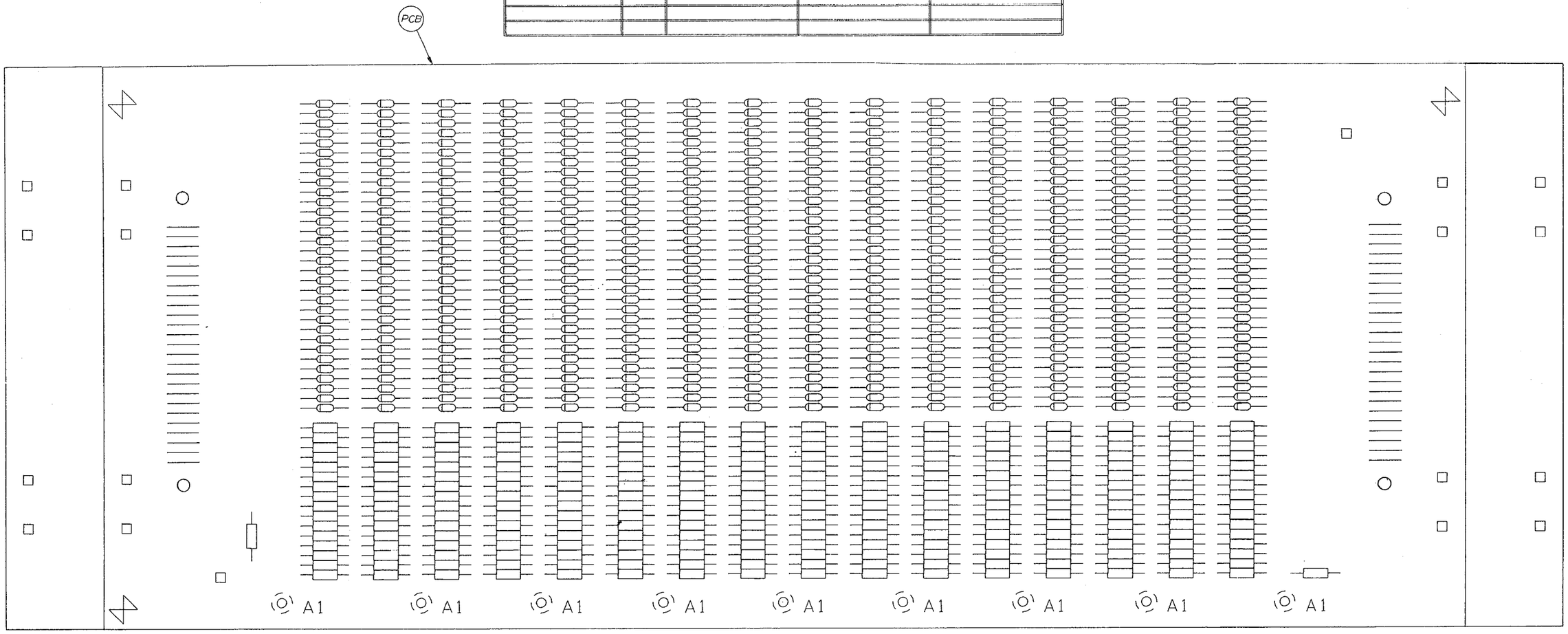
NOTE:
SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

REF. ASSEMBLY MD XXX M			TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010	DIGIVUE® DISPLAY / MEMORY UNITS OWENS-ILLINOIS
E				
D	ECO# 37	12/14/75 FP		
C	REVISED ECO # 24	6/6/75 MRC	MATERIAL	TITLE COMPONENT ASSEMBLY
B	ECO# 14	3/7/75 FP		DRAWN CHECKED APPROVED DATE
A	REVISED PER PRE-PRODUCTION	9/4/74 FP		SCALE 2X DRAWING NO DD340C0400D
NO	REVISIONS	DATE BY		

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
UNM'K	512	DIODE		1N4938/ITT2002
UNM'K	258	RES. 25W 5.6K 10%	A.B.	RCR07
PCB	1	PRINTED CKT. BRD.		CD340D0500E
A1	9	2-56 THD. BUSH.	PEM	Y-1316ET



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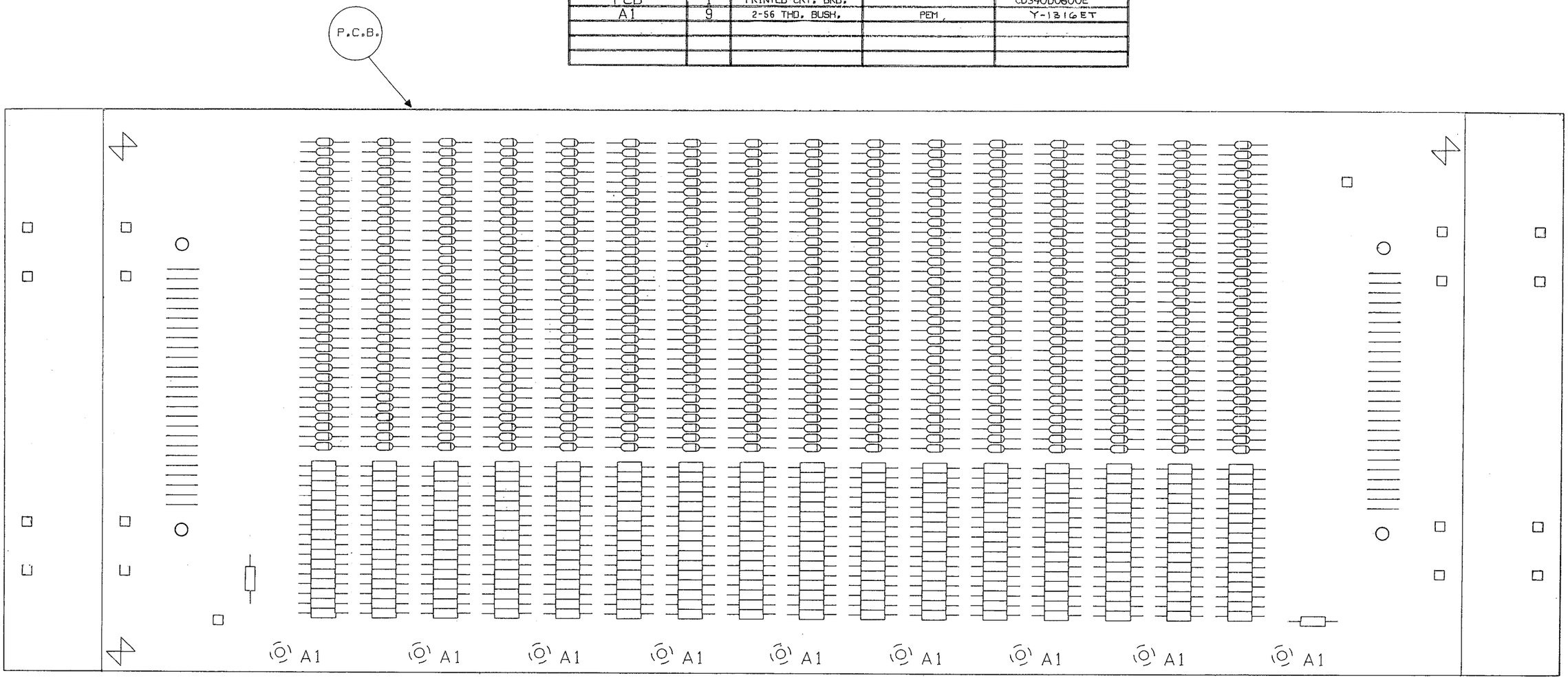
NOTE:
SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

REF. ASSEMBLY MDXXXM				TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .030	DIGIVUE® DISPLAY/MEMORY UNITS OWENS-ILLINOIS
E					
D	E.C.#37	7/14/78	FP		
C	Revised ECO# 24			MATERIAL	TITLE COMPONENT ASSEMBLY
B	ECO#16	5/10/78	FP		DRAWN RSM CHECKED SRS APPROVED JKW DATE 7-7-78
A	REVISED PCE PRE-PRODUCTION	5/4/78	FP		SCALE 2X DRAWING NO. D0340C0500D
NO	REVISIONS	DATE	BY		

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
UNM'K	512	DIODE		1N4938/1TT2002
UNM'K	258	RES.25W 5.6K 10%	A.B.	RCR07
PCB	1	PRINTED CKT. BRD.		CD340D0600E
A1	9	2-56 THD. BUSH.	PEM	Y-1816ET



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Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function

NOTE:
SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

NO	REVISIONS	DATE	BY
E			
D	ECO# 37	12/14/76	FP
C	REVISED ECO# 24	6/6/75	MRB
B	ECO# 14	3/17/75	FD
A	REVISED PER PRE-PRODUCTION	9/9/74	FD

REF. ASSEMBLY MDXXXM

TOLERANCES
ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL

DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS

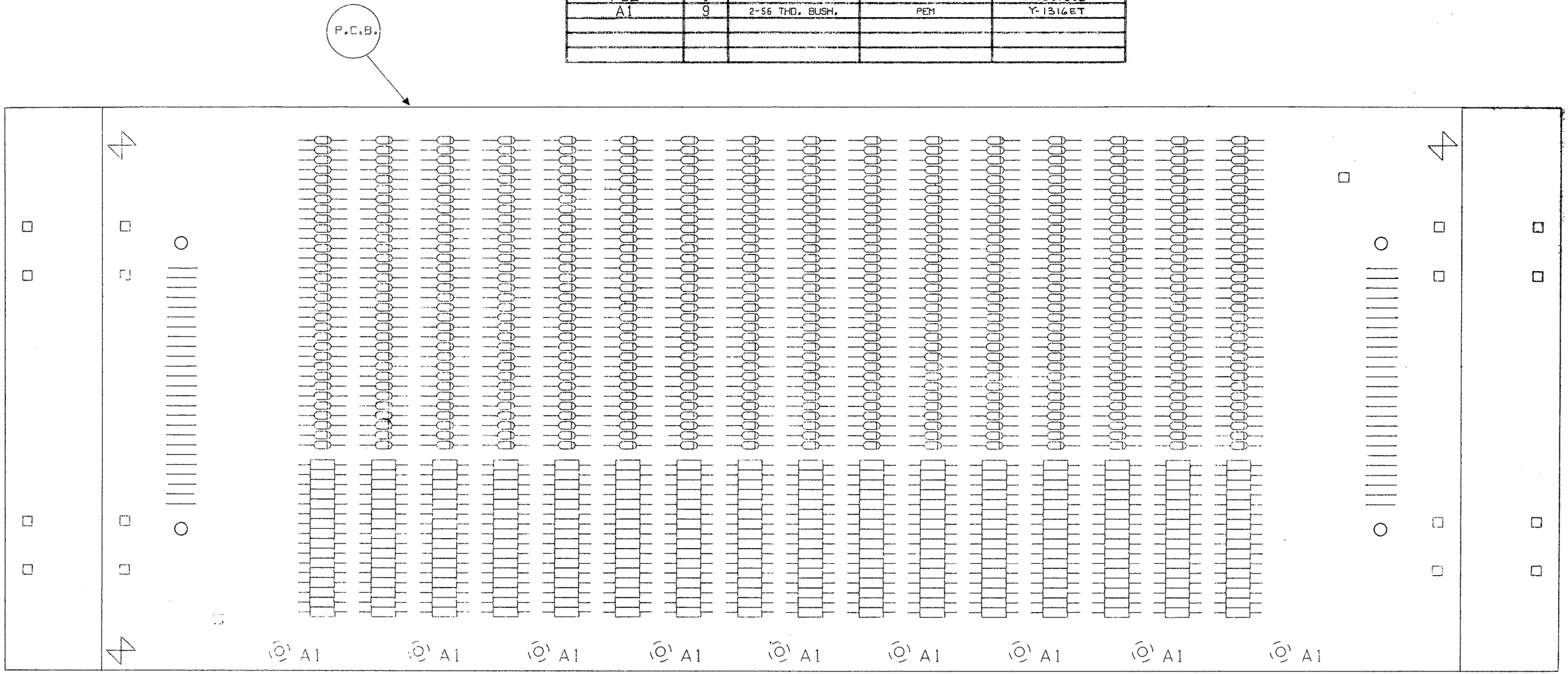
TITLE COMPONENT ASSEMBLY

DRAWN	CHECKED	APPROVED	DATE
E.G.M.	[illegible]	[illegible]	7/74

SCALE 2X

DRAWING NO. DD340C0600D

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
UNM'K	512	DIODE		1N4938/ITT2002
UNM'K	256	RES. .25W 5.6K 10%	A.B.	RCR07
PCB	1	PRINTED CKT. BRD.		CD340D0700E
A1	9	2-56 THD. BUSH.	PEM	Y-1316ET



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NOTE:
SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300

NO	REVISIONS	DATE	BY
E			
D	ECO# 37	12/4/15	FP
C	Revised ECO# 24	6/4/15	MRL
B	ECO#14	3/17/15	FP
A	REVISED PER PRE-PRODUCTION	3/4/15	FP

REF. ASSEMBLY MDXXXM

TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL

DIGIVUE®
DISPLAY/MEMORY UNITS
OWENS-ILLINOIS

TITLE COMPONENT ASSEMBLY

DRAWN	CHECKED	APPROVED	DATE
E.G.M.			7/1/

SCALE 2X

DRAWING NO. DD340C0700E

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
C1C2	2	CAP. , uf at 12v	CENTRALAB	XXUKI2-104
C3	1	" 220uf at 10v	I.E.C.	TAD220TH 10
CR1-64, CR66-76	79	DIODE		IN4938 or ITT2002
CR65	1	"	GE	A 114E
R1- R16	16	RESISTOR, 25W 56K 10%	A.B	RCR07
R17, 28-31, R38-41	9	" " 100Ω 5%	"	"
R18	1	" " 330Ω "	"	"
R21-23, R32, 33	5	" " 390Ω "	"	"
R19	1	" " 39Ω "	"	"
R20, 24-27, 34-37	9	" " 68Ω "	"	"
U1, U2	2	I.C. 74145	T.I.	SN 74145
Q1	1	TRANSISTOR	MOTOROLA/FAIR.	2N4402
Q2	1	"	" "	2N5682
Q3-Q10	8	"	MOTOROLA	2N5551
T1-T2	2	TRANSFORMER	POTTER	7220-1005

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
A1	4	4-40 THREADED BUSH.	USECO	9004B-No PLATE
A2	2	SPACER, TEFLON	SEAL ECTRO	119 0739
PCB	1	PRINTED CIRCUIT BD.		CD340D0800

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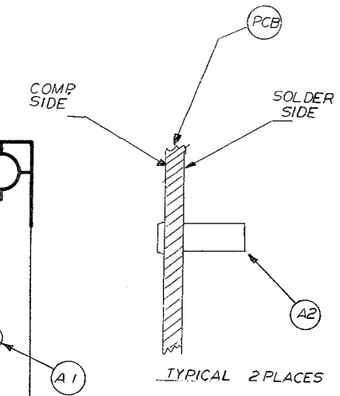

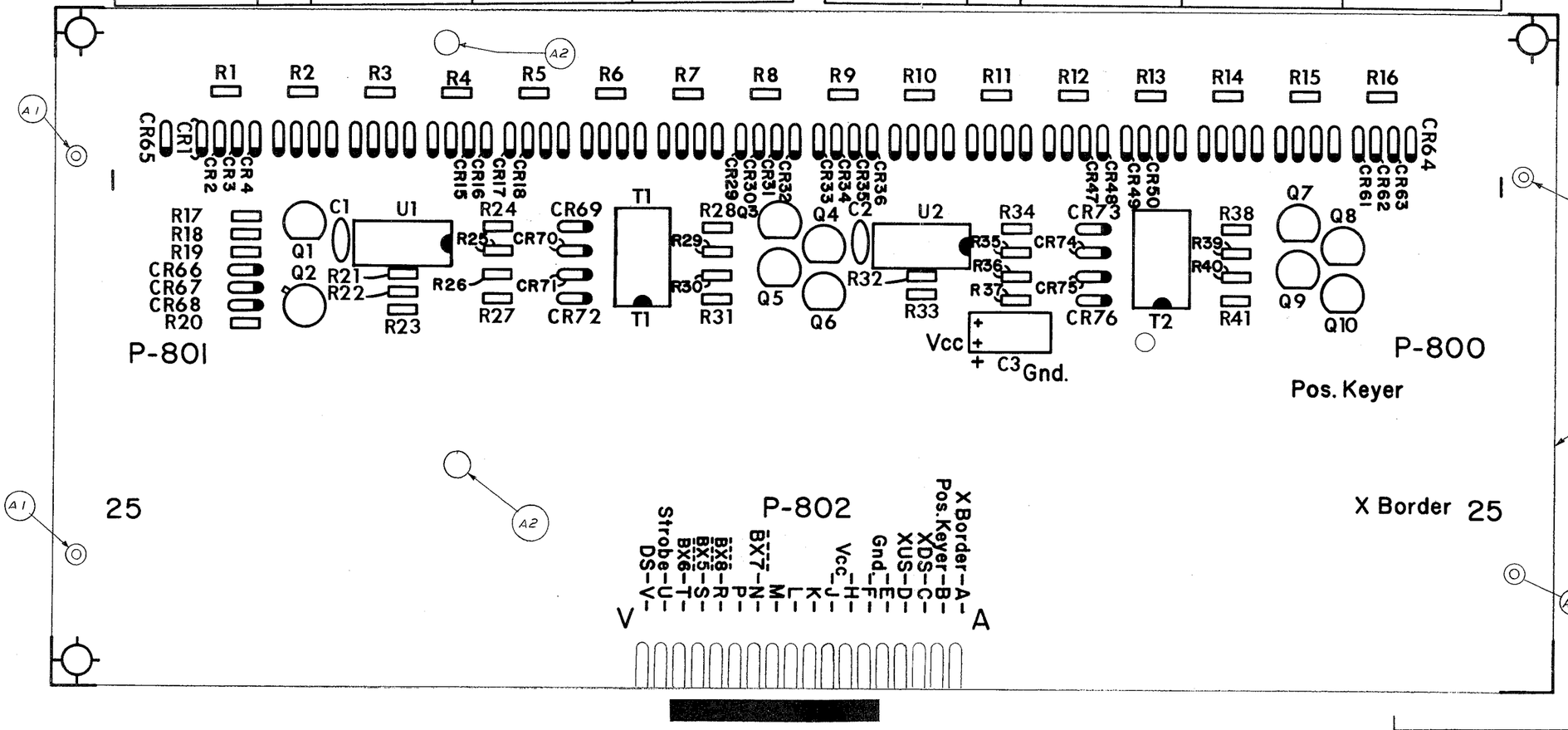

NOTE:
1. ZINC PLATING PER ZINC DICHROMATE SPEC 210M0200A TYPE II, CLASS 2
2. SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

REF. ASSEMBLY MDXXXM				TOLERANCES UNLESS OTHERWISE SPECIFIED ALL FRACTIONAL DIMENSIONS ± 1/32 AND ALL DECIMAL DIMENSIONS ± .010	DIGIVUE® DISPLAY / MEMORY UNITS OWENS-ILLINOIS	
E						
D						
C	ECO#32	10/31/75	FP	MATERIAL	TITLE COMPONENT ASSEMBLY	
B	REVISED ECO#24	4/4/75	IRC		DRAWN EJH/MK	CHECKED JAB
A	REVISED PER PRE-PRODUCTION	3/9/74	FP		SCALE 2X	DRAWING NO. D340C0800C
NO.	REVISIONS	DATE	BY			

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
C1,C2	2	CAP. .1uf at 12v	CENTRALAB	XXUK12-104
C3	1	" 220uf at 10 v	I.E.C.	TAD220THIO
CR1-64, CR66-76	79	DIODE		1N4938 or ITT2002
CR65	1	"	GE	A 114E
R1- R16	16	RESISTOR,.25W 5.6K 10%	A.B.	RCR07
R17,28-31, R38-41	9	" " 100Ω 5%	"	"
R18	1	" " 330Ω "	"	"
R21-23 R32, 33	5	" " 390Ω "	"	"
R19	1	" " 39Ω "	"	"
R20, 24-27, 34-37	9	" " 68Ω "	"	"
U1, U2	2	I.C. 74145	T.I.	SN 74145
Q1	1	TRANSISTOR	MOTOROLA/FAIR.	2N4402
Q2	1	"	" "	2N5682
Q3-Q10	8	"	MOTOROLA	2N5551
T1-T2	2	TRANSFORMER	POTTER	7220-1005

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
A1	4	4-40 THREADED BUSH.	USECO	9004B-No PLATE
A2	2	SPACER, TEFLON	SEAL ECTRO	119-0739
PCB	1	PRINTED CIRCUIT BD.		CD340D0900

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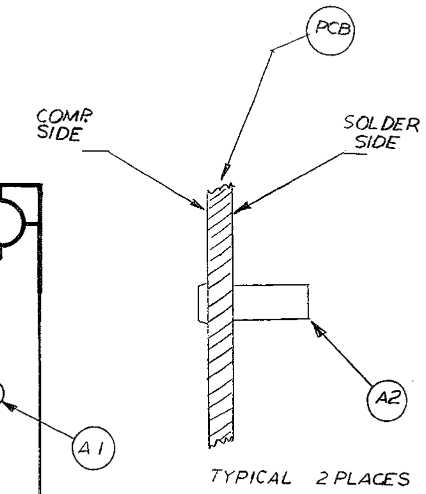
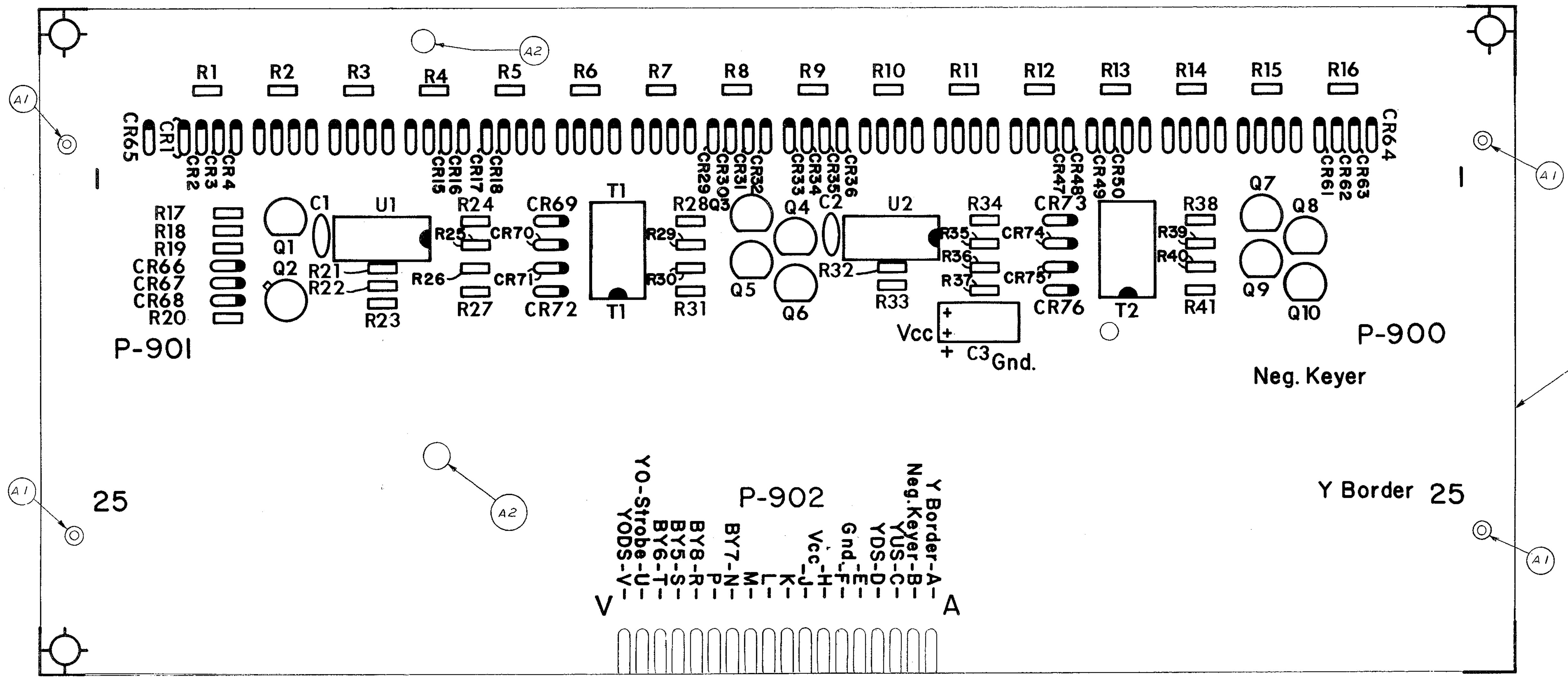




Note:
1. Zinc plating per zinc dichromate spec 210m0200A Type II, class 2
2. See general purchased component requirements 220m0300

REF. ASSEMBLY MDXXXM			
E			
D			
C	ECO#32	10/13/75	FP
B	Revised ECO #24	6/6/75	MRG
A	REVISED PER PRE-PRODUCTION	9/9/74	FP
NO	REVISIONS	DATE	BY

TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL

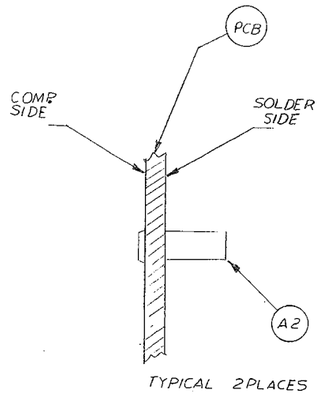
DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS

TITLE COMPONENT ASSEMBLY

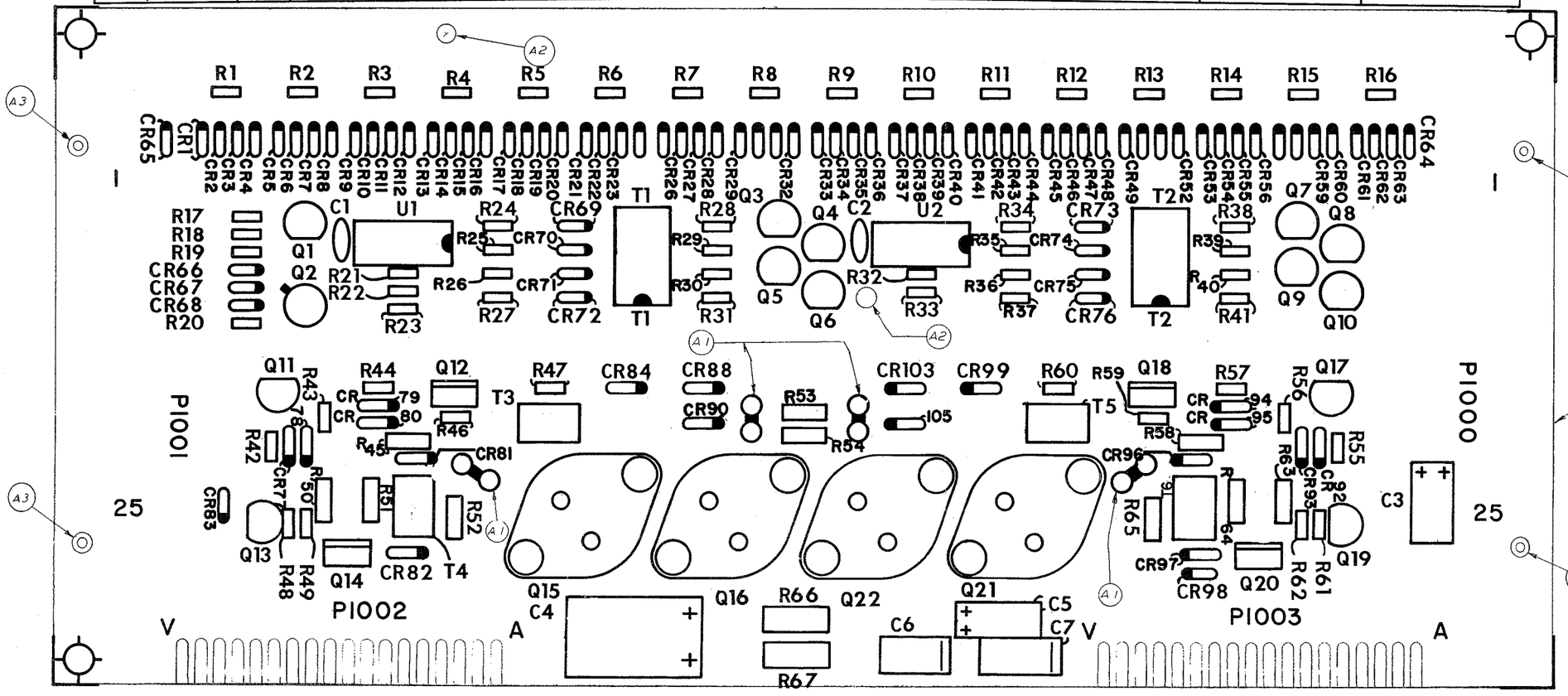
DRAWN	CHECKED	APPROVED	DATE
[signature]	[signature]	[signature]	6/74
SCALE 2X	DRAWING NO. DD340C0900C		

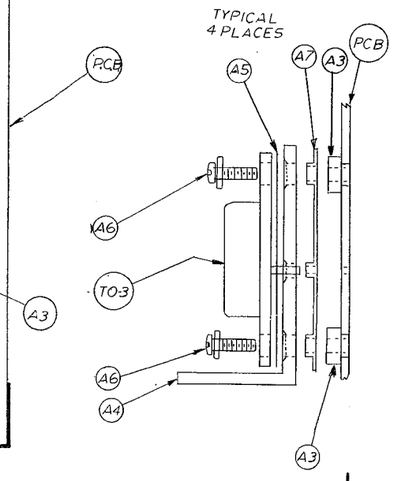
SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
C1,C2	2	CAP. .1uf at 12v	CENTRALAB	XXUK12-104
C3,C5	2	" 220uf at 10v	I.E.C.	TAD220TH10
C4	1	" 32uf at 250v	MEPCO	C436AR/M32
C6,C7	2	" .33uf at 100v	I.E.C.	MDEF 334MB1A
CR-81,90,9C,105	4	DIODE	C[illegible]	AIKL C,R AIIE
CR1-64,66-80,92-95	83	DIODE		IN4938 or ITT2002
CR65	1	"	GE	A 114E
CR-82-84,88,97-99,103	8	"	"	DT230HI
R1 - R16	16	RESISTOR,25W 56K 10%	A.B.	RCR07
R17,28-31,R38-41,99,97	11	" " 100Ω 5%	"	"
R18	1	" " 330Ω "	"	"
R21-23,56,32,33,42,43,55	9	" " 390Ω "	"	"
R19	1	" " 39Ω "	"	"
R20,24-27,34-37R46,	13	" " 68Ω "	"	"
R49,59,62		" " " "	"	"
R44,48,57,61	4	" " 33Ω "	"	"
R45,50,58,63	4	" .5W 1Ω "	"	RCR20
R51,64	2	" " 68Ω 10%	"	"
R52,65	2	" " 1.6Ω 5%	"	"
R66,67	2	" 1W 39K 10%	"	RCR32

SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
Q1,11,13,17,19	5	TRANSISTOR	MOT./FAIR.	2N4402
Q2	1	"	"	2N5682
Q3-10	8	"	MOTOROLA	2N5551
Q12,14,18,20	4	"	G.E.	D45C3
Q15,16,21,22	4	"	T.I.	EP1337
U1,U2	2	I.C. 74145	"	SN74145
A1	4	WIRE #18AWG, 3" BLACK		UL STYLE 1007 PREFUSED
A2	2	SPACER, TEFLON	SEAL ECTRO	119-0739
A3	12	4-40 THREADED BUSH.	USECO	90048-No PLATE
A4	1	HEAT SINK		D 340M2600-B
A5	4	KAPTON INSULATOR	THERMALLOY	43-03-9
A6	8	4-40x 1/2" SCREW, PAN HD., SEMS, WITH INT TOOTH LOCKWASHER ZINC PLATE		
A7	4	LEAD SPACER	ROBINSON ELECT.	RC-T03062-1
T1,2	2	TRANSFORMER	POTTER	7220-1005
T3-6	4	"	"	7120-1019
R53,54	2	RESISTOR,5W 2.7Ω 5%	A.B.	RCR20



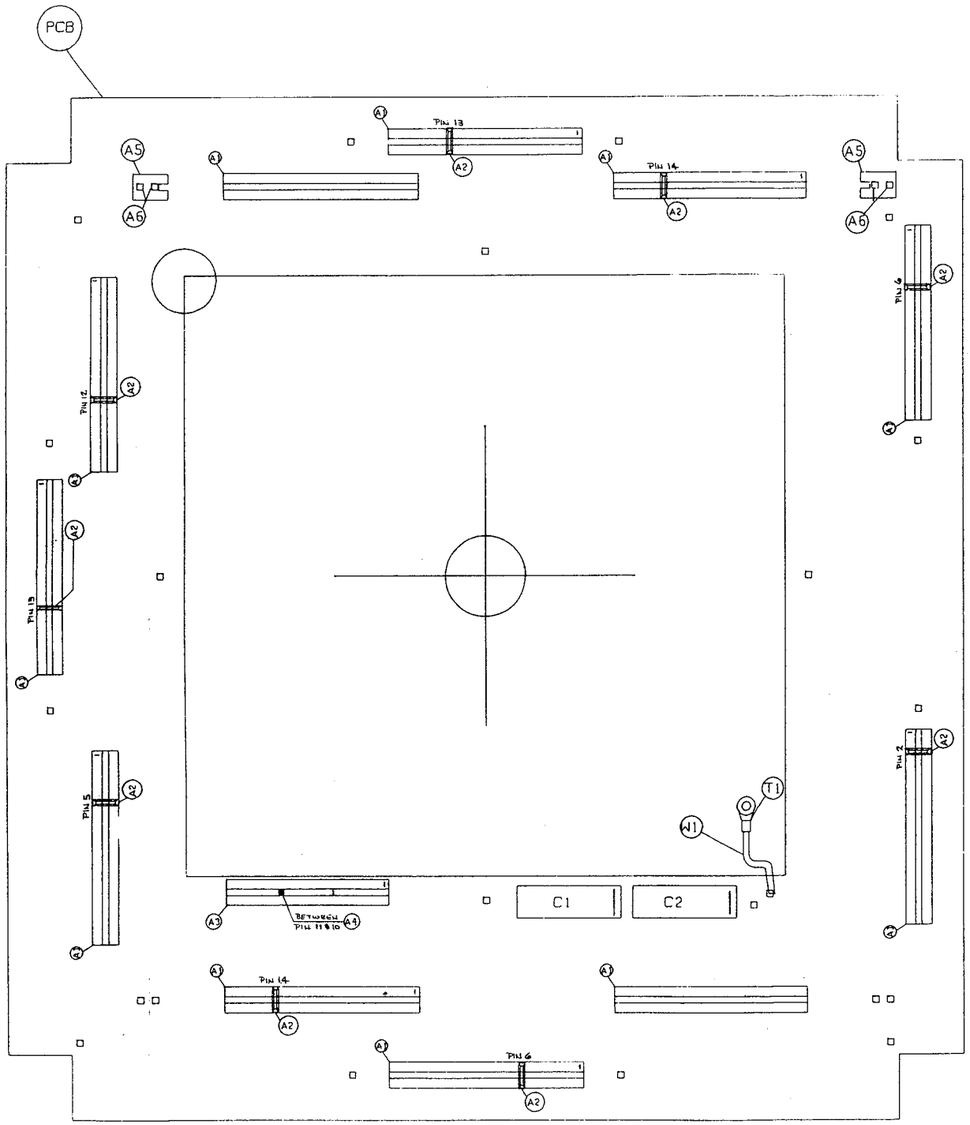
TYPICAL 2 PLACES





NOTE P.
1. ZINC PLATING PER ZINC DICHROMATE SPEC 210M0200A TYPE II, CLASS 2
2. SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

REF. ASSEMBLY MDXXXM			TOLERANCES	DIGIVUE® DISPLAY / MEMORY UNITS OWENS-ILLINOIS
E	ECO# 32	10/14/75 FP	ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .015	
D	REVISED PER ECO#25 & 24	6/6/75		
C	ECO# 10 & ECO#3	5/11/75 FP	MATERIAL	TITLE COMPONENT ASSEMBLY
B	ECO# 3	3/20/74 WB		DRAWN GM · CHECKED · APPROVED JC Cm · DATE 7-74
A	REVISED PER PRE-PRODUCTION	2/15/74 FP		SCALE 2X · DRAWING NO DD340C1000E
NO	REVISIONS	DATE BY		



SYMBOL	QTY	DESCRIPTION	VENDOR	PART NO.
A1	11	CONNECTOR, 18PIN	AMP	3-583486-3
A2	9	KEY, POLARIZING	AMP	583714-2
A3	1	CONNECTOR, 15PIN	AMP	583660-2
A4	1	KEY, POLARIZING	AMP	530030-1
P.C.B.	1	PRINTED CKT BD.		DD340D1100-A
C1, C2	2	CAP. 2.2UF/250V	MEPCO	C280MAE/A2M2
W1	1	WIRE, BLK. 2IN.	PREFUSED 18 AWG	UL STYLE 1007
T1	1	SOLDER LUG	ZERICK	501-6
A5	2	CARD GUIDE	AMP	583671-1
A6	4	SREW #2X1/4 PAN		
		HD. -ZINC PLATE -THREAD		
		CUTTING, POINT TYPE BF, BT OR F		

Owens-Illinois makes no warranty, expressed or implied, as to the correctness or completeness of the information presented in this document

Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.

NOTE:
ZINC PLATING PER ZINC DICHROMATE SPEC 210M0200A TYPE II CLASS 2.

NOTE:
SEE GENERAL PURCHASED COMPONENT REQUIREMENTS 220M0300.

NO	REVISIONS	DATE	BY
C	REVISED ECO #24	6/15/82	RCA
B	REVISED PER PRE-PRODUCTION	3/3/82	FP
A	REVISED REF LOCATIONS AND REMOVED (1) KEY	9/24/81	RCA

REF. ASSEMBLY MDXXM

TOLERANCES UNLESS FRACTIONS OR FRACTIONAL DIMENSIONS ± .010

MATERIAL

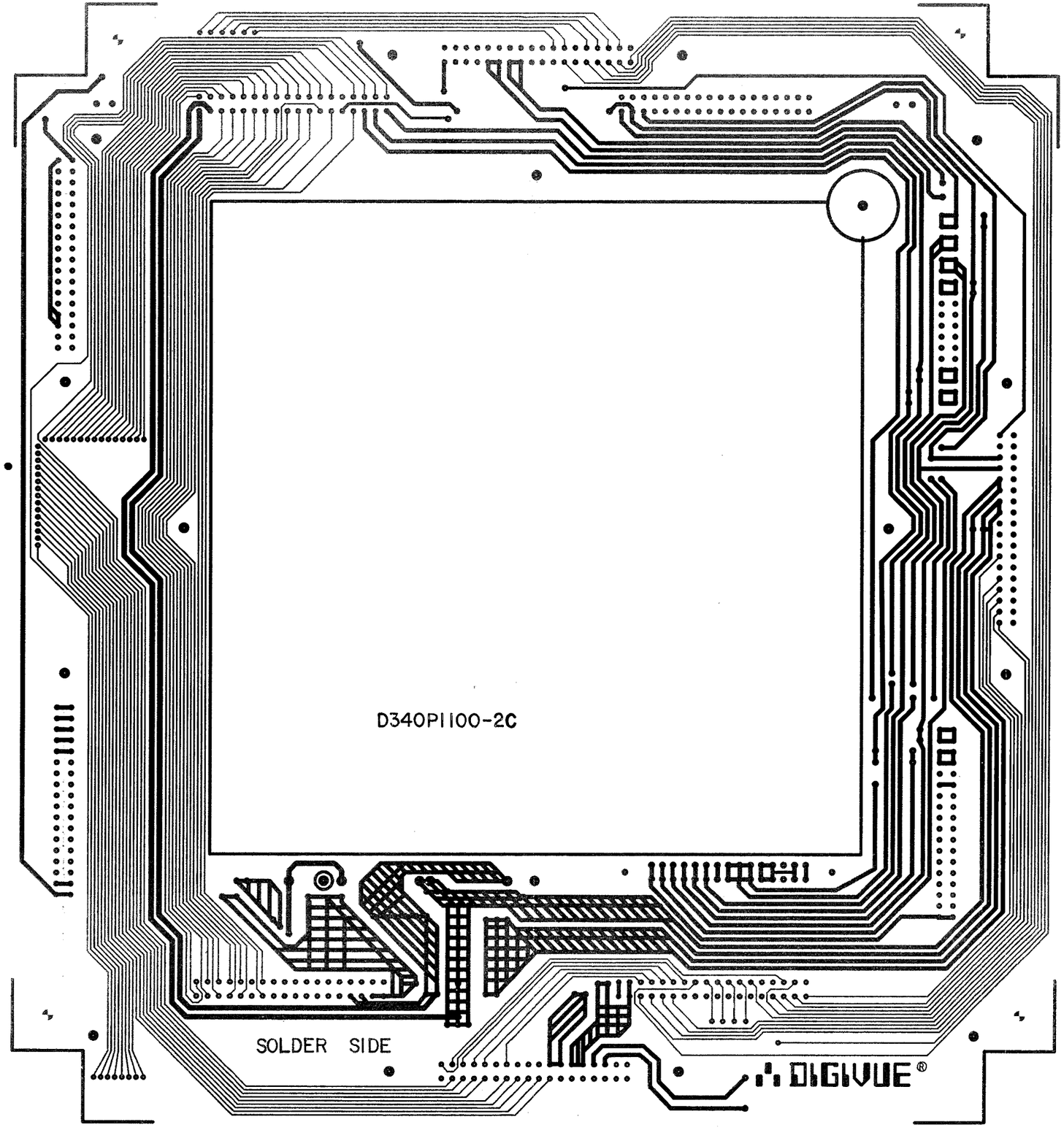
DIGIVUE®
DISPLAY/MEMORY UNITS
OWENS-ILLINOIS

TITLE COMPONENT ASSEMBLY

DRAWN	CHECKED	APPROVED	DATE
EGM			7/79

SCALE 2X

DRAWING NO. DD340C1100E



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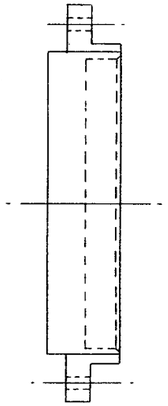
Components listed on this document are for engineering reference only. Manufactured units may contain listed components or O-I recognized substitutes of an equal or better specification for the circuit function.

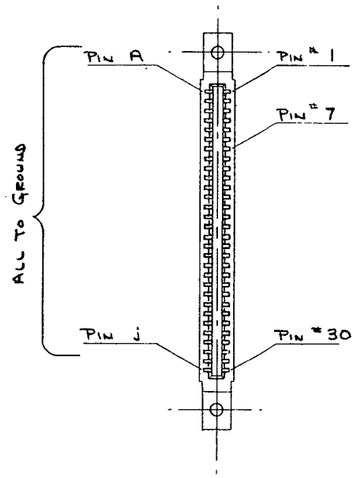
1. AUTOMATIC DISPLAY INITIATED BULK ERASE EVENTS WILL OCCUR 30 MIN. ± 7.5 MIN. AFTER RECEIPT OF LAST WRITE OR ERASE REQUEST.

2. CONTROL LINES

C0	C1	
H	H	SUSTAIN
L	H	ERASE
H	L	WRITE
L	L	BULK ERASE

3. ALL OTHER DATA LINES ARE POSITIVE LOGIC.





* INNER CONTACT POLARIZING KEY BETWEEN PINS 6 & 7

PIN # 1	—	GND. (OUTPUT)
2	—	+5 Vcc (OUTPUT)
3	—	SYNC
4	—	STATUS
5	—	WRITE
* 6	—	BULK ERASE
7	—	ERASE
8	—	X0
9	—	X3
10	—	X5
11	—	X7
12	—	X6
13	—	X8
14	—	C0
15	—	C1
16	—	DO NOT USE
17	—	Y1
18	—	X1
19	—	X2
20	—	X4
21	—	Y8
22	—	Y3
23	—	Y4
24	—	Y6
25	—	Y7
26	—	Y2
27	—	Y5
28	—	Y0
29	—	FRAME GND
30	—	GND

AMP TWIN LEAF PRINTED CIRCUIT EDGE CONNECTOR WITH CRIMP ON, SNAP IN CONTACTS ON .100" CENTERS

HOUSING	—	# 1-583718-3	(1)
CONTACT	—	# 583854-5	(60)
KEY PLUG	—	# 583274-1	(1)

1 REQ'D.

REF. ASSEMBLY MD XXXM			
E			
D			
C			
B			
A			
NO	REVISIONS	DATE	BY

TOLERANCES ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL PURCHASE

DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS

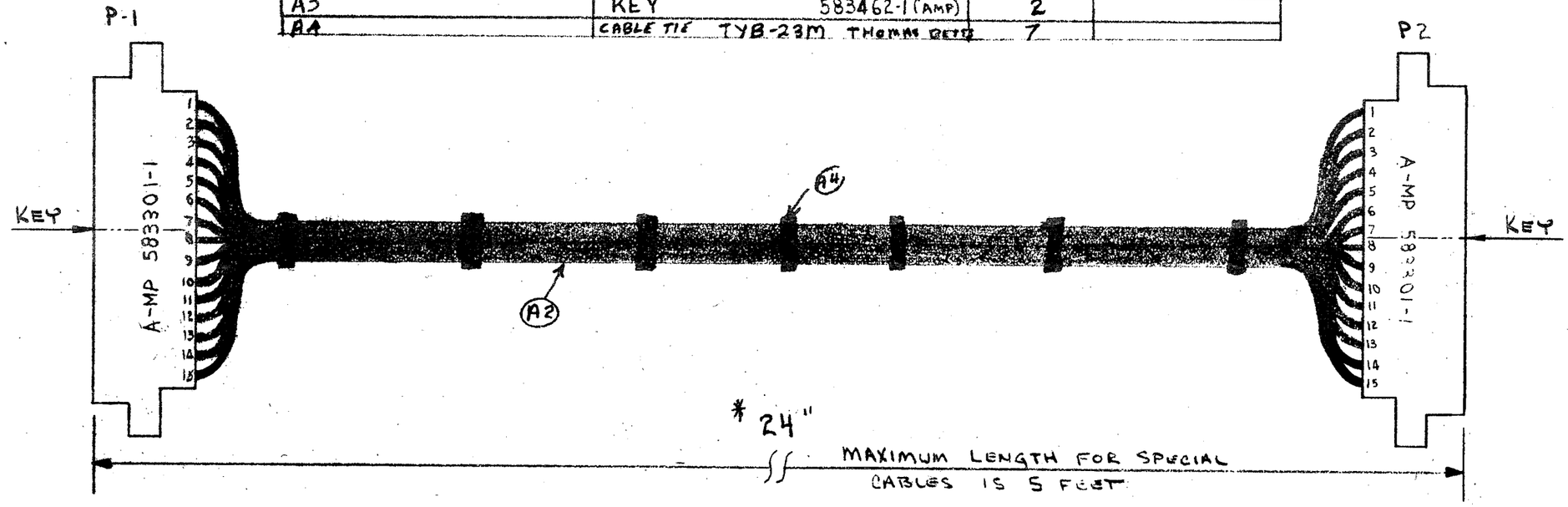
TITLE CONNECTOR, LOGIC

DRAWN	CHECKED	APPROVED	DATE
M.R.G.			

SCALE 1:1

DRAWING NO. BD340M5000A

SYMBOL	DESCRIPTION	QUANTITY	O.I. PART No.
P1, P2	CONNECTOR 583301-1 (AMP)	2	
A1	PIN 583362-4 (AMP)	30	
A2	WIRE ~ BRAND-REX OR ALPHA U.L. STYLE 1007	15	
A3	KEY 583462-1 (AMP)	2	
A4	CABLE TIE TYB-23M THOMAS BETTS	7	



TERMINATION LIST

COLOR				
WHT/BLACK	P1 PIN 1	-SENSE		P2 PIN 1
WHT/ORANGE	" 2	+SENSE		" 2
GREEN	" 3	GND (CHASSIS)		" 3
BLUE	" 4	VCC (+5VDC)		" 4
BLUE	" 5	VCC (+5VDC)		" 5
BLACK	" 6	GND		" 6
BLACK	" 7	GND		" 7
BLACK	P1 PIN 8	GND (-VSS)		P2 PIN 8
WHT/RED	" 9	VSB (+165VDC)	+38 (+120 at front of [illegible] for 20 sec)	" 9
RED	" 10	VSS (+125VDC)	+85 to +105	" 10
VIOLET	" 11	VAX (POS)	+65 to +85	" 11
WHT/YELLOW	" 12	VAX (COM)		" 12
BROWN	" 13	VAY (COM)		" 13
WHT/BROWN	" 14	VAY (NEG)	-65 to -85	" 14
YELLOW	P1 PIN 15	VSC +8	+8	P2 PIN 15

A3 - KEY - BETWEEN PINS 7+8 IN P1+P2

NOTE: TWIST WIRE PAIR (P1-1 to P2-1) and (P1-2 to P2-2)
MAKE TWIST WIRES 2" LONGER

*24" LENGTH CABLE - STANDARD
16" LENGTH CABLE - TERMINAL USE

REF. ASSEMBLY			
E			
D			
C			
B			
A	REVISED PER NEW DWG	5/21/74	MRG
NO	REVISIONS	DATE	BY

TOLERANCES
ALLOWABLE VARIATIONS ON FRACTIONAL DIMENSIONS IS ± .010

MATERIAL

DIGIVUE®
DISPLAY / MEMORY UNITS
OWENS-ILLINOIS 5/21/74

TITLE CABLE, POWER MDXXX-M

DRAWN	CHECKED	APPROVED	DATE
M.R.G.			

SCALE: ~

DRAWING NO. BP340M1400 A