MOTOROLA, INC.

CONTROL SYSTEMS DIVISION

PHOENIX, ARIZONA

Technical Memo

TM-CP8-1

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ABSTRACT: MDP-1000 Instruction Repertoire

MIC-1 INSTRUCTION REPERTOIRE

SYMBOL	MEANING
( )	CONTENT OF
P	IDENTIFIES AN ARBITRARY MEMORY LOCATION
P + 1	IDENTIFIES MEMORY LOCATION SEQUENTIAL TO P
CAS	COMPILER/ASSEMBLY SYSTEM
R	PROGRAMMABLE HARDWARE REGISTER

REGISTER	CODE	REGISTER	CODE
A	0	P	4
X	1	B	5
Y	2	YY	6
Z	3	ZZ	7

EXCEPT FOR SKIP INSTRUCTIONS WHICH ARE SINGLE BYTE, ALL OTHER INSTRUCTIONS ARE FORMED BY TWO BYTES. TWO TECHNIQUES MAY BE USED TO FORM THESE INSTRUCTIONS (1) IMMEDIATE AND (2) SHARED. WITH THE IMMEDIATE TECHNIQUE TWO SEQUENTIAL BYTES "P" AND "P+1" ARE USED. WITH THE SHARED TECHNIQUE, THE TWO BYTES ARE SEPARATED, IE, BYTE "P" EXISTS IN THE PRIMARY PROGRAM BUT THE SECOND BYTE EXISTS IN A DEDICATED MEMORY AREA AND MAY BE SHARED. THERE IS NO DIFFERENCE IN EXECUTION TIME BETWEEN IMMEDIATE AND SHARED TECHNIQUES.

FOUR INSTRUCTION SETS MAY EMPLOY THE SHARED TECHNIQUE: REGISTER CHANGE, ARITHMETIC/LOGICAL, PULSE/SHIFT, AND AUGMENTED MEMORY. SIXTEEN (16) DEDICATED MEMORY LOCATIONS ARE ALLOWED FOR EACH OF THESE INSTRUCTION SETS.

SHARED CAS/ASM CLASS

CAS	(P)	INSTRUCTION SET
A* [R],B	020 - 037	ARITHMETIC/LOGICAL
R* TR,F	040 - 057	REGISTER CHANGE
P* SS,R	060 - 077	PULSE/SHIFT
GN* LL	200 - 217	AUGMENTED MEMORY

P IDENTIFIES:

1. INSTRUCTION SET
2. * ABSOLUTE ADDRESS OF SECOND BYTE. THE SECOND BYTE IS DEFINED UNDER THE IMMEDIATE CLASS INSTRUCTIONS AS P + 1.

TYPICAL INSTRUCTIONS - AN ASTERISK FOLLOWING OP CODE IN CAS DEFINES SHARED COMMANDS

* ABSOLUTE ADDRESS FOR SECOND BYTE UNDER AUGMENTED MEMORY INSTRUCTION SET IS 100 - 117.

AUGMENTED MEMORY, IMMEDIATE CLASS

(ALL REGISTERS PERMITTED EXCEPT B AS INDICATED)

N: ADDRESS DELTA, N = 0, 2, 4, 6

EOA: EFFECTIVE OPERAND ADDRESS

I: INDIRECT ADDRESS MODE

T: INDEX (TAG) REGISTER

0 - NO INDEX 2. TAG WITH Y

1 - TAG WITH X 3. TAG WITH Z

CAS	(P)	(P+1)	INSTRUCTION	OPERATION FULL REG.	OPERATION PARTIAL REG
GN LR GN LR,T	00 N/2	T0R	LOAD DIRECT	$(EOA)_{0-7} \rightarrow (R)_{0-7}$ $C \rightarrow (L)_{8-11}$ $*EOA \rightarrow (B)_{0-11}$	$(EOA)_{0-3} \rightarrow (R)_{8-11}$ $(R)_{0-7} \rightarrow (R)_{0-7}$ $EOA \rightarrow (B)_{0-11}$
GN LR,I GN LR,T,I	00 N/2	T4R	LOAD INDIRECT	*B SEL: NOT APPLICABLE	
GN SR GN SR	00 N/2	T3R	STORE DIRECT	$(R)_{0-7} \rightarrow (EOA)_{0-7}$ $(R)_{0-11} \rightarrow (R)_{0-11}$ $EOA \rightarrow (B)_{0-11}$	$(R)_{8-11} \rightarrow (EOA)_{0-3}$ $(R)_{0-11} \rightarrow (R)_{0-11}$ $EOA \rightarrow (B)_{0-11}$
GN SR,I GN SR,T,I	00 N/2	T7R	STORE INDIRECT	B SEL: NOT PERMITTED	
GN AR GN AR,T	00 N/2	T2R	ADD DIRECT	$(R)_{0-11} + (EOA)_{0-7} \rightarrow (R)_{0-11}$ $EOA \rightarrow (B)_{0-11}$	$(R)_{8-11} + (EOA)_{0-3} \rightarrow (R)_{8-11}$ $(R)_{0-7} \rightarrow (R)_{0-7}$ $EOA \rightarrow (B)_{0-11}$
GN AR,I GN AR,T,I	00 N/2	T6R	ADD INDIRECT	B SEL: NOT PERMITTED	
GN ZR GN ZR,T	00 N/2	T1R	STORE AND CLEAR DIRECT	$(R)_{0-7} \rightarrow (EOA)_{0-7}$ $0 \rightarrow (R)_{0-11}$ $EOA \rightarrow (B)_{0-11}$	$(R)_{8-11} \rightarrow (EOA)_{0-3}$ $0 \rightarrow (R)_{8-11}$ $(R)_{0-7} \rightarrow (R)_{0-7}$ $EOA \rightarrow (B)_{0-11}$
GN ZR,I GN ZR,T,I	00 N/2	T5R	STORE AND CLEAR INDIRECT	B SEL: $0 \rightarrow (EOA)_{0-7}$ $0 \rightarrow (B)_{0-11}$	

DIRECT MODE

$$EOA = N + (T)_{0-11}$$

INDIRECT MODE

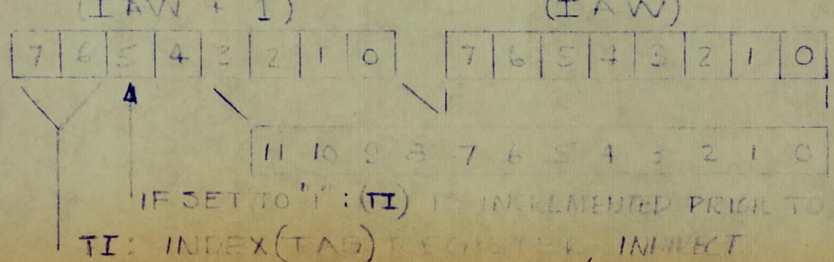
	7	6	5	4	3	2	1	0
IAW								
IAW + 1	7	6	5	4	3	2	1	0

1. LOCATION OF IAW (INDIRECT ADDRESS WORD) IS GIVEN BY:

$$IAW = N + (T)_{0-11}$$

2. LOCATION OF EOA IS GIVEN BY:

$$EOA = PARTIAL\ EOA + (TI)_{0-11}$$



IF SET TO '1': (TI) IS INCREMENTED PRIOR TO EOA DERIVATION

TI: INDEX (TAG) REGISTER, INDIRECT

0 - NO INDEX 2 - TAG WITH Y

1 - TAG WITH X 3 - TAG WITH Z

ARITHMETIC/LOGICAL IMMEDIATE CLASS

(ALL REGISTERS PERMITTED EXCEPT B)

CAS	(P)	(P+1)	INSTR.		OPERATION FULL REG.	OPERATION PARTIAL REG.
A NR B	004	02R	AND	∧	$(R)_{0-7}$ ☐ $(B)_{0-7} \rightarrow (R)_{0-7}$	$(R)_{8-11}$ ☐ $(B)_{0-3} \rightarrow (R)_{8-11}$
A OR B	004	06R	OR	∨	$0 \rightarrow (R)_{8-11}$	$(R)_{0-7} \rightarrow (R)_{0-7}$
A XR B	004	04R	EXCLOR	⊻	$(B)_{0-11} \rightarrow (B)_{0-11}$	$(B)_{0-11} \rightarrow (B)_{0-11}$
A AR B	004	30R	ADD	+	$(R)_{0-11}$ ☐ $(B)_{0-11} \rightarrow (R)_{0-11}$	
A SR B	004	20R	SUBTRACT	−	$(B)_{0-11} \rightarrow (B)_{0-11}$	
A NR P+2	004	03R	AND	∧	$(R)_{0-7}$ ☐ $(P+2)_{0-7} \rightarrow (R)_{0-7}$	$(R)_{8-11}$ ☐ $(P+2)_{0-3} \rightarrow (R)_{8-11}$
A OR P+2	004	07R	OR	∨	$0 \rightarrow (R)_{8-11}$	$(R)_{0-7} \rightarrow (R)_{0-7}$
A XR P+2	004	05R	EXCLOR	⊻	$(P+2)_{0-7} \rightarrow (B)_{0-7}$	$(P+2)_{0-7} \rightarrow (B)_{0-7}$
A AR P+2	004	31R	ADD	+	$0 \rightarrow (B)_{8-11}$	$0 \rightarrow (B)_{8-11}$
A SR P+2	004	21R	SUBTRACT	−		
A LR B	004	10R	LOAD		$(B)_{0-7} \rightarrow (R)_{0-7}$	$(B)_{0-3} \rightarrow (R)_{8-11}$
					$0 \rightarrow (R)_{8-11}$	$(R)_{0-7} \rightarrow (R)_{0-7}$
					$(B)_{0-11} \rightarrow (B)_{0-11}$	$(B)_{0-11} \rightarrow (B)_{0-11}$
A LR P+2	004	11R	LOAD		$(P+2)_{0-7} \rightarrow (R)_{0-7}$	$(P+2)_{0-3} \rightarrow (R)_{8-11}$
					$0 \rightarrow (R)_{8-11}$	$(R)_{0-7} \rightarrow (R)_{0-7}$
					$(P+2)_{0-7} \rightarrow (B)_{0-7}$	$(P+2)_{0-7} \rightarrow (B)_{0-7}$
					$0 \rightarrow (B)_{8-11}$	$0 \rightarrow (B)_{8-11}$
A ZR	004	00R	ZERO		$0 \rightarrow (R)_{0-11}$	$0 \rightarrow (R)_{8-11}$
						$(R)_{0-7} \rightarrow (R)_{0-7}$

REGISTER CHANGE IMMEDIATE CLASS

(ALL REGISTERS PERMITTED)

CAS	(P)	(P+1)	INSTR.		OPERATION FULL REG.	OPERATION PARTIAL REG.
R TR, F	010	3FR	TRANSFER	→	$(R)_{0-11}$ ☐ $(F)_{0-11}$	$(R)_{8-11}$ ☐ $(F)_{8-11}$
R DR, F	010	2FR	DECREMENT	-1	*	
R IR, F	010	1FR	INCREMENT	+1		
R LR, F	010	0FR	ADD LINK	+L		

R: ORIGIN REGISTER
F: DESTINATION REGISTER

*SPECIAL CASE
R DR, R
$-1 \rightarrow (B)_{0-11}$

PULSE SHIFT INSTRUCTIONS

SHIFT MODE — ALL REGISTER FUNCTIONS EXCEPT T AND S)

CAS	(F)	(F+1)	INSTRUCTION	OPERATION FULL REG	OPERATION PARTIAL REG
P SS,K	014	00R	SHIFT	0 → [7 ··· 0] → [L] →	0 → [11 ··· 8] → [L] →
P SC,K	014	02R	CIRCULATE	→ [7 ··· 0] → [L] →	0 → [11 ··· 8] → [L] →
P SL,K	014	01R	CIRCULATE THRU LINK	→ [7 ··· 0] → [L]	0 → [11 ··· 8] → [L] →
P SI,K	014	04R	SERIAL DATA IN	SERIAL DATA IN → [7 ··· 0] → [L] →	NOT APPLICABLE
P SØ,K	014	12R	SERIAL DATA OUT	→ [7 ··· 0] → [L] → ; SERIAL DATA OUT	NOT APPLICABLE
P SIØ,K	014	14K	SERIAL DATA IN AND OUT	SERIAL DATA IN ← [7 ··· 0] → [L] → ; SERIAL DATA OUT	NOT APPLICABLE

PULSE MODIFY

CAS	(F)	(F+1)	INSTRUCTION	OPERATION
P PR	014	200	RESET LINK	0 ⟶ L
P PS	014	201	SET LINK	1 ⟶ L
P PF	014	202	GENERATE FAP (FUNCTION ADDRESS PULSE).	PULSE → I/Ø "FUNCTION ADDRESS" LINE B_{0-11} → I/Ø DATA BUS
P PT	014	203	GENERATE TOP (TRANSFER OUT PULSE)	PULSE → I/Ø "TRANSFER OUT" LINE $(E)_{0-11}$ → I/Ø DATA BUS
P PI	014	204	GENERATE TIP (TRANSFER IN PULSE)	PULSE → I/Ø "TRANSFER IN" LINE I/Ø DATA BUS → $(E)_{0-11}$
P PB	014	205	TRANSFER E TO B	$(E)_{8-11}$ → $(B)_{0-3}$ 0 → $(B)_{4-11}$
P PQ	014	207	INTERROGATE INTERRUPT	IF KIC INTERRUPT SET 0012 → $(P)_{0-11}$ (HIGHEST PRIORITY) IF I/Ø INTERRUPT SET 00[0] → $(P)_{0-11}$
P PE	014	206	LOAD MEMORY ADDRESS EXTENDER	$(E)_{0-2}$ → $(E)_{0-2}$ $(F)_{0-11}$ → $(E)_{0-11}$

PAGE 2048 WORDS

E	1	2	3	4	5	6	7	8
1	X	X						
2	X		X					
3	X			X				
4	X				X			
5	X					X		
6	X						X	
7	X							X

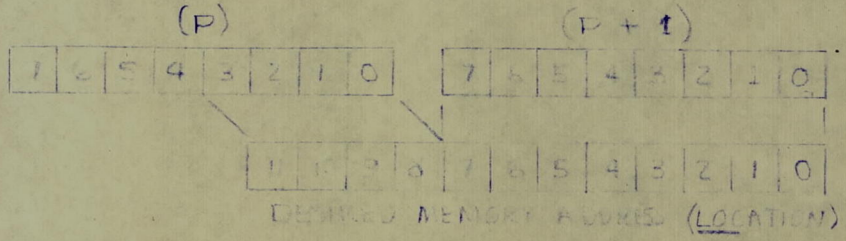
← "SYSTEM RESET" SETS THIS CONDX.

SKIPS

CAS	(P)	TEST	SKIP TO	CAS	(P)	TEST	SKIP TO
K F0	100	NØP	P + 1				
K F2	101	I/O FALSE	P + 3	K N2	111	NOT ZERO	P + 3
K F4	102	"	P + 5	K N4	112	"	P + 5
K F6	103	"	P + 7	K N6	113	"	P + 7
K T2	121	I/O TRUE	P + 3	K Z2	131	ZERO	P + 3
K T4	122	"	P + 5	K Z4	132	"	P + 5
K T6	123	"	P + 7	K Z6	133	"	P + 7
K R2	105	LINK RESET	P + 3	K M2	115	MINUS	P + 3
K R4	106	"	P + 5	K M4	116	"	P + 5
K R6	107	"	P + 7	K M6	117	"	P + 7
K S2	125	LINK SET	P + 3	K P2	135	PLUS	P + 3
K S4	126	"	P + 5	K P4	136	"	P + 5
K S6	127	"	P + 7	K P6	137	"	P + 7

JUMP AND LOAD B / STORE B INSTRUCTIONS

CAS	(P)	(P + 1)	INSTRUCTION	OPERATION
J LOC	140 - 157	000 - 377	JUMP	$LOC \longrightarrow (P)_{0-11}$
E LOC	160 - 177	000 - 377	LOAD B EXTENDED	$(LOC)_{0-7} \longrightarrow (B)_{0-7}$ $(LOC + 1)_{0-3} \longrightarrow (B)_{8-11}$
S LOC	300 - 317	000 - 377	STORE B NO INDEX	$(B)_{0-7} \longrightarrow (LOC)_{0-7}$
S LOC,X	320 - 337	000 - 377	STORE B X INDEX	$(B)_{0-7} \longrightarrow [LOC + (X)_{8-11}]_{0-7}$
L LOC	340 - 357	000 - 377	LOAD B NO INDEX	$(LOC)_{0-7} \longrightarrow (B)_{0-7}$ $0 \longrightarrow (B)_{8-11}$
L LOC,X	360 - 377	000 - 377	LOAD B X INDEX	$[LOC + (X)_{8-11}]_{0-7} \longrightarrow (B)_{0-7}$ $0 \longrightarrow (B)_{8-11}$



LOC DEFINES DESIRED OCTAL MEMORY ADDRESS (LOCATION)

I.E., 0000 THRU 3777

LINK

THE LINK REGISTER IS SET OR RESET WHENEVER AN ARITHMETIC OR SHIFT INSTRUCTION IS EXECUTED. FOR ARITHMETIC OPERATIONS (ADD, SUBTRACT, INCREMENT, DECREMENT) THE LINK IS SET "TRUE" IF A CARRY OCCURS OUT OF BIT 7 OF THE ADDER AND IS SET "FALSE" IF NO CARRY OCCURS. FOR SHIFT OPERATIONS SEE DIAGRAMS SHOWN UNDER "SHIFT" IN MAIN DATA CLASS.

PLUS

THE PLUS REGISTER IS SET "TRUE" IF BIT 7 OF THE ADDER RESULT IS A "0" AND VICE VERSA.

MINUS

THE MINUS REGISTER IS SET "TRUE" IF BIT 7 OF THE ADDER RESULT IS A "1" AND VICE VERSA.

ZERO

THE ZERO REGISTER IS SET "TRUE" IF BITS 7 THRU 0 OF THE ADDER RESULT ARE ALL "0's". IF ANY OR ALL OF THE BITS ARE "1's" THE ZERO REGISTER IS SET "FALSE".

PARTIAL ASCII CODE

A	301	R	322	0	260
B	302	S	323	1	261
C	303	T	324	2	262
D	304	U	325	3	263
E	305	V	326	4	264
F	306	W	327	5	265
G	307	X	330	6	266
H	310	Y	331	7	267
I	311	Z	332	8	270
J	312			9	271
K	313			SPACE	240
L	314			LF	212
M	315			CR	215
N	316			RUB OUT	377
O	317			BELL	207
P	320				
Q	321				